Automotive PSoC™ 4: PSoC™ 4000S family

Based on Arm® Cortex®-M0+ CPU

General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. The PSoC™ 4000S product family is a member of the PSoC™ 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CAPSENSE™) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC™ 4000S products will be upward compatible with members of the PSoC™ 4 platform for new applications and design needs.

Features

- Automotive Electronics Council (AEC) AEC-Q100 Qualified
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 32 KB of flash with read accelerator
  - Up to 4 KB of SRAM
- Programmable analog
  - Single-slope 10-bit ADC function provided by capacitance sensing block
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep low-power mode
- Programmable digital
  - Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs
- Low-power 1.71-V to 5.5-V operation
  - Deep Sleep mode with operational analog and 2.5 µA digital system current
- Capacitive sensing
  - Capacitive sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (>5:1) and water tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- Serial communication
  - Two independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I2C, SPI, or UART functionality
- LCD drive capability
  - LCD segment drive capability on GPIOs
- Timing and pulse-width modulation
  - Five 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, Edge, and pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications
- Up to 24 programmable GPIO pins
  - 24-pin QFN, 28-pin SSOP
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable

Features

- PSoC™ Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)
  - Applications programming interface (API) component for all fixed-function and programmable peripherals
- Industry-standard tool compatibility
  - After schematic entry, development can be done with Arm®-based industry-standard development tools
- Temperature range
  - A-Grade: –40°C to +85°C
  - E-Grade: –40°C to +125°C
  - S-Grade: –40°C to +105°C

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firmware that enables debugging. Thus firmware control of debugging cannot be over-ridden without erasing the firmware thus providing security.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. All programming, debug, and test interfaces are disabled when maximum device security is enabled. Therefore, PSoC™ 4000S, with device security enabled, may not be returned for failure analysis. This is a trade-off the PSoC™ 4000S allows the customer to make.

1 Functional definition

1.1 CPU and memory subsystem

1.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4000S is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions

1.2.2 Clock system

The PSoC™ 4000S clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4000S consists of the internal main oscillator (IMO), internal low-frequency oscillator (ILO), a 32 kHz Watch Crystal Oscillator (WCO) and provision for an external clock. Clock dividers are provided to generate clocks for peripherals on a fine-grained basis. Fractional dividers are also provided to enable clocking of higher data rates for UARTs.

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are eight clock dividers for the PSoC™ 4000S, two of those are fractional dividers. The 16-bit capability allows flexible generation of fine-grained frequency values, and is fully supported in PSoC™ Creator.

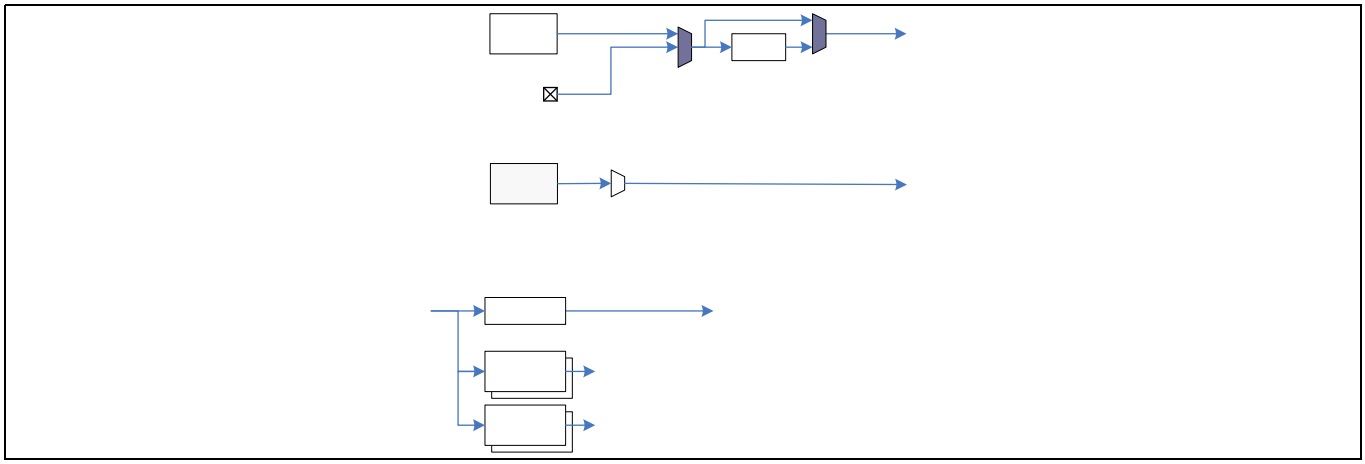


Figure 1 PSoC™ 4000S MCU Clocking architecture

1.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4000S. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is ±2%.

1.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

1.2.5 Watch Crystal Oscillator (WCO)

The PSoC™ 4000S clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

1.5 Fixed function digital blocks

1.5.1 Timer/Counter/PWM (TCPWM) Block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to

1.6 GPIO

The PSoC™ 4000S has up to 24 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width (less for Ports 2 and 3). During power-on and reset, the blocks are forced to the disabled state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC™ 4000S).

1.7 Special function peripherals

1.7.1 CAPSENSE™

CAPSENSE™ is supported in the PSoC™ 4000S through a capacitive sigma-delta (CSD) block that can be connected to any pins through an analog multiplex bus via analog switches. CAPSENSE™ function can thus be provided on any available pin or group of pins in a system under software control. A PSoC™ Creator component is provided for the CAPSENSE™ block to make it easy for the user.

Shield voltage can be driven on another analog multiplex bus to provide water-tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input. Proximity sensing can also be implemented.

The CAPSENSE™ block has two IDACs, which can be used for general purposes if CAPSENSE™ is not being used (both IDACs are available in that case) or if CAPSENSE™ is used without water tolerance (one IDAC is available).

The CAPSENSE™ block also provides a 10-bit Slope ADC function, which can be used in conjunction with the CAPSENSE™ function.

The CAPSENSE™ block is an advanced, low-noise, programmable block with programmable voltage references and current source ranges for improved sensitivity and flexibility. It can also use an external reference voltage. It has a full-wave CSD mode that alternates sensing to VDDA and Ground to null out power-supply related noise.

1.7.2 LCD segment drive

The PSoC™ 4000S has an LCD controller, which can drive up to 4 commons and 20 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as Digital Correlation and PWM. Digital Correlation pertains to modulating the frequency and drive levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal to zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays. PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

2 Pinouts

Table 1 provides the pin list for PSoC™ 4000S for the 24-pin QFN and 28-pin SSOP packages. All port pins support GPIO.

Table 1 Automotive PSoC™ 4000S 24-pin QFN and 28-pin SSOP pin list

24-QFN		28-SSOP	
Pin	**Name**	**Pin**	**Name**
13	P0.0	19	P0.0
14	P0.1	20	P0.1
		21	P0.2
		22	P0.3
15	P0.4		
16	P0.5		
17	P0.6	23	P0.6
		24	P0.7
18	XRES	25	XRES
19	VCCD	26	VCCD
20	VSSD	27	VSS
21	VDD	28	VDD
22	VSSA		
		1	P1.0
		2	P1.1
23	P1.2	3	P1.2
24	P1.3	4	P1.3
		5	P1.4
1	P1.7	6	P1.7
2	P2.0		
3	P2.1		
		7	P2.4
		8	P2.5
4	P2.6	9	P2.6
5	P2.7	10	P2.7
6	P3.0	11	P3.0
		12	P3.1
7	P3.2	13	P3.2
8	P3.3	14	P3.3
9	P4.0	15	P4.0
10	P4.1	16	P4.1
11	P4.2	17	P4.2
12	P4.3	18	P4.3

Descriptions of the pin functions are as follows:

VDDD: Power supply for the digital section.

VDDA: Power supply for the analog section.

VSSD, VSSA: Ground pins for the digital and analog sections respectively.

VCCD: Regulated digital supply (1.8 V ±5%)

VDD: On some packages, VDDA and VDDD are shorted inside and brought out as a single power supply

VSS: On some packages, VSSA and VSSD are shorted inside and brought out as a single ground

Pinouts

Port/ pin	Analog	Smart I/O	Alternate function 1	Alternate function 2	Alternate function 3	Deep Sleep 1	Deep Sleep 2
P2.4		prgio[0].io[4]	tcpwm.line[0]:1				scb[1].spi_select1:1
P2.5		prgio[0].io[5]	tcpwm.line_compl[0]:1				scb[1].spi_select2:1
P2.6		prgio[0].io[6]	tcpwm.line[1]:1				scb[1].spi_select3:1
P2.7		prgio[0].io[7]	tcpwm.line_compl[1]:1			lpcomp.comp[0]:1	
P3.0		prgio[1].io[0]	tcpwm.line[0]:0	scb[1].uart_rx:1		scb[1].i2c_scl:2	scb[1].spi_mosi:0
P3.1		prgio[1].io[1]	tcpwm.line_compl[0]:0	scb[1].uart_tx:1		scb[1].i2c_sda:2	scb[1].spi_miso:0
P3.2		prgio[1].io[2]	tcpwm.line[1]:0	scb[1].uart_cts:1		cpuss.swd_data	scb[1].spi_clk:0
P3.3		prgio[1].io[3]	tcpwm.line_compl[1]:0	scb[1].uart_rts:1		cpuss.swd_clk	scb[1].spi_select0:0
P3.4		prgio[1].io[4]	tcpwm.line[2]:0		tcpwm.tr_in[6]		scb[1].spi_select1:0
P3.5			tcpwm.line_compl[2]:0		tcpwm.tr_in[7]		scb[1].spi_select2:0
P3.6			tcpwm.line[3]:0		tcpwm.tr_in[8]		scb[1].spi_select3:0
P3.7			tcpwm.line_compl[3]:0		tcpwm.tr_in[9]	lpcomp.comp[1]	
P4.0	csd.vref_ext			scb[0].uart_rx:0	tcpwm.tr_in[10]	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshieldpads			scb[0].uart_tx:0	tcpwm.tr_in[11]	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmodpad			scb[0].uart_cts:0		lpcomp.comp[0]:0	scb[0].spi_clk:0
P4.3	csd.csh_tank			scb[0].uart_rts:0		lpcomp.comp[1]:0	scb[0].spi_select0:0

4 Development support

The PSoC™ 4000S family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **PSoC™ 4 MCU** webpage to find out more.

4.1 Documentation

A suite of documentation supports the PSoC™ 4000S family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

Software user guide: A step-by-step guide for using PSoC™ Creator. The software user guide shows you how the PSoC™ Creator build process works in detail, how to use source control with PSoC™ Creator, and much more.

Component datasheets: The flexibility of PSoC™ allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

Application notes: PSoC™ application notes discuss a particular application of PSoC™ in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

Technical reference manual: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC™ device, including a complete description of all PSoC™ registers. The TRM is available in the Documentation section at **PSoC™ 4 MCU** webpage**.**

4.2 Online

In addition to print documentation, the PSoC™ forums connect you with fellow PSoC™ users and experts in PSoC™ from around the world, 24 hours a day, 7 days a week.

4.3 Tools

With industry standard cores, programming, and debugging interfaces, the PSoC™ 4000S family is part of a development tool ecosystem. Visit us at **PSoC™ Creator** webpage for the latest information on the revolutionary, easy to use PSoC™ Creator IDE, supported third party compilers, programmers, debuggers, and development kits.

5 Electrical specifications

5.1 Absolute maximum ratings

5.2 Device level specifications

All specifications are valid for –40°C T_A 85°C for A grade devices and –40°C T_A 105°C for S grade devices,

Table 3 DC specifications *(continued)*

Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.2	2.0	mA	Max is at 105°C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	2.4	4.0		Max is at 105°C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	4.6	5.9		Max is at 105°C and 5.5 V
Sleep Mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup WDT, and Comparators on	–	1.1	1.6	mA	6 MHz, Max is at 105°C and 5.5 V
SID25	I_{DD20}	I^2C wakeup, WDT, and Comparators on	–	1.4	1.9		12 MHz, Max is at 105°C and 5.5 V
Sleep Mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	I_{DD23}	I^2C wakeup, WDT, and Comparators on	–	0.7	0.9	mA	6 MHz, Max is at 105°C
SID28A	I_{DD23A}	I^2C wakeup, WDT, and Comparators on	–	0.9	1.1	mA	12 MHz, Max is at 105°C and 5.5 V
Deep Sleep Mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID31	I_{DD26}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 105°C and 3.6 V
Deep Sleep Mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID34	I_{DD29}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 105°C
Deep Sleep Mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID37	I_{DD32}	I^2C wakeup and WDT on	–	2.5	60	µA	Max is at 105°C
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	Max is at 105 °C

Table 4 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V_{DD} 5.5
SID49[2]	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID50[2]	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		–

Note
2. Guaranteed by characterization.

5.2.1 GPIO

Table 5 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}[3]	Input voltage high threshold	0.7 V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 V_{DDD}		CMOS Input
SID241	V_{IH}[3]	LVTTL input, V_{DDD} < 2.7 V	0.7 V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 V_{DDD}		–
SID243	V_{IH}[3]	LVTTL input, V_{DDD} 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} –0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} –0.5	–	–		I_{OH} = 1 mA at 3 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[4]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDD} 2.7 V
SID68[4]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[4]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[4]	I_{DIODE}						

Table 6 GPIO AC specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V V_{DDD} 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V V_{DDD} 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V V_{DDD} 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V V_{DDD} 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V V_{DDD} 5.5 V	–	–	48		90/10% V_{IO}

5.2.2 XRES

Table 7 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V						

Table 8 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83[5]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[5]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

5.3 Analog peripherals

Table 9 Comparator DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	–
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		–
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		–
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD}-0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD}-1.15		V_{DDD} ≥ 2.2 V at –40 °C
SID88	C_{MRR}	Common mode rejection ratio	50	–	–	dB	V_{DDD} ≥ 2.7V
SID88A	C_{MRR}	Common mode rejection ratio	42	–	–		V_{DDD} ≤ 2.7V
SID89	I_{CMP1}	Block current, normal mode	–	–	400	µA	–
SID248	I_{CMP2}	Block current, low power mode	–	–	100		–
SID259	I_{CMP3}	Block current in ultra low-power mode	–	6	28		V_{DDD} ≥ 2.2 V at –40°C
SID90	Z_{CMP}	DC Input impedance of comparator	35	–	–	MΩ	–

Table 10 Comparator AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID91	TRESP1	Response time, normal mode, 50 mV overdrive	–	38	110	ns	–
SID258	TRESP2	Response time, low power mode, 50 mV overdrive	–	70	200		–
SID92	TRESP3	Response time, ultra-low power mode, 200 mV overdrive	–	2.3	15	µs	V_{DDD} ≥ 2.2 V at –40°C

5.3.1 CSD

Table 11 CSD and IDAC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details /conditions
SYS.PER#3	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25 °C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25 °C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator.
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#15A	VREF_EXT	External voltage reference for CSD and Comparator	0.6		V_{DDA} - 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID.CSD#16	IDAC1IDD	IDAC1 (7-bits) block current	–	–	1750	µA	–
SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	–
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ±5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	V_{DDA} - 0.06 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	–
SID310	IDAC1INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID311	IDAC2DNL	DNL	–1	–	1	LSB	
SID312	IDAC2INL	INL	–2	–	2	LSB	INL is ±5.5 LSB for V_{DDA} < 2 V
SID313	SNR	Ratio of counts of finger to noise. Guaranteed by characterization	5	–	–	Ratio	Capacitance range of 5 to 35 pF, 0.1-pF sensitivity. All use cases. V_{DDA} > 2 V.
SID314	IDAC1CRT1	Output current of IDAC1 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID314A	IDAC1CRT2	Output current of IDAC1(7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID314B	IDAC1CRT3	Output current of IDAC1(7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.

SID314C	IDAC1CRT12	Output current of IDAC1 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID314D	IDAC1CRT22	Output current of IDAC1(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID314E	IDAC1CRT32	Output current of IDAC1(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315	IDAC2CRT1	Output current of IDAC2 (7 bits) in low range	4.2	–	5.4	µA	LSB = 37.5-nA typ.
SID315A	IDAC2CRT2	Output current of IDAC2 (7 bits) in medium range	34	–	41	µA	LSB = 300-nA typ.
SID315B	IDAC2CRT3	Output current of IDAC2 (7 bits) in high range	275	–	330	µA	LSB = 2.4-µA typ.
SID315C	IDAC2CRT12	Output current of IDAC2 (7 bits) in low range, 2X mode	8	–	10.5	µA	LSB = 75-nA typ.
SID315D	IDAC2CRT22	Output current of IDAC2(7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600-nA typ.
SID315E	IDAC2CRT32	Output current of IDAC2(7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8-µA typ.
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5-nA typ.
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300-nA typ.
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4-µA typ.
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	–
SID322	IDACMIS-MATCH1						

Table 11 CSD and IDAC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details /conditions
SID322B	IDACMIS-MATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4-µA typ.
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	µs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap.



Table 20 LCD Direct Drive DC specifications[6]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 4 segments. 50 Hz. 25°C.
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 4 segments. 50 Hz. 25°C.

Table 21 LCD Direct Drive AC specifications[7]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

5.5 Memory

Table 22 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and program voltage	1.71	–	5.5	V	–

Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress (an Infineon company) prefix		–
4	Architecture	4	PSoC™ 4
A	Family	0	4000 Family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	LQ/LD	QFN
		PV	SSOP
F	Temperature range	I	Industrial
		A	Automotive (AEC-Q100: –40°C to +85°C)
		S	Automotive (AEC-Q100: –40°C to +105°C)
		E	Automotive (AEC-Q100: –40°C to +125°C)
S	Silicon family	S	PSoC™ 4A-S1, PSoC™ 4A-S2
		M	PSoC™ 4A-M
		L	PSoC™ 4A-L
		BL	PSoC™ 4A-BLE
XYZ	Attributes code	000-999	Code of feature set in the specific family
XX	Fab/Assembly location	Non KA	Initial Assembly location
		Blank	

The following is an example of a part number:

Example

™

7 Packaging

The Automotive PSoC™ 4000S will be offered in 24-QFN and 28-SSOP packages.

Table 36 provides the package dimensions and Infineon drawing numbers.

Table 36 Package list

Spec ID	Package	Description	Package drawing
BID34	24-pin QFN	4 × 4 × 0.6 mm height, 2.75 × 2.75 mm EPAD (Sawn)	002-18982
BID28	28-pin SSOP	210 Mils O28.21	51-85079

Table 37 Package thermal characteristics

Parameter	Description	Package	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature		For A-grade devices	–40	25	85	°C
			For S-grade devices	–40	25	105	
T_J	Operating junction temperature		For A-grade devices	–40	–	100	°C
			For S-grade devices	–40	–	120	
T							

7.1 Package diagrams

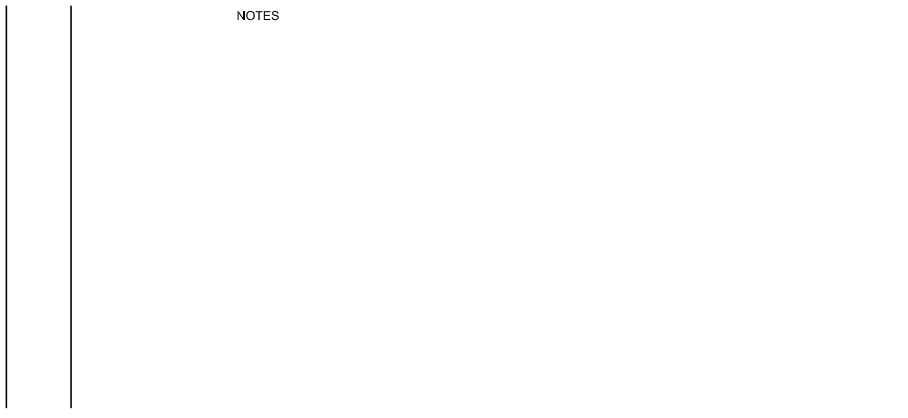


Figure 4 24-pin QFN package outline (PG-VQFN-24)

8 Acronyms

Table 40 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharg.0004s6r.4(dT*.00011 TcT)53.803Fta4rf311c thumegic unit

Table 40 Acronyms used in this document *(continued)*

Acronym	Description
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array



Acronyms

PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC™	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit

Table 40 Acronyms used in this document *(continued)*

Acronym	Description
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

9 Document conventions

9.1 Units of measure

Table 41 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
k	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
M	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
W	ohm
pF	pico(mill)(micmp)- TcnsmV

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