Automotive PSoC™ 4: PSoC™ 4100S Plus

Based on Arm® Cortex®-M0+ CPU

General description

PSoC™ 4 is a scalable and reconfigurable platform architecture for a family of programmable embedded system controllers with an Arm® Cortex®-M0+ CPU while being AEC-Q100 compliant. It combines programmable and reconfigurable analog and digital blocks with flexible automatic routing. PSoC™ 4100S Plus is a member of the PSoC™ 4 platform architecture. It is a combination of a microcontroller with standard communication and timing peripherals, a capacitive touch-sensing system (CAPSENSE™) with best-in-class performance, programmable general-purpose continuous-time and switched-capacitor analog blocks, and programmable connectivity. PSoC™ 4100S Plus products will be upward compatible with members of the PSoC™ 4 platform for new applications and design needs.

Features

- Automotive Electronics Council (AEC) AEC-Q100 Qualified
- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0+ CPU
  - Up to 128 KB of flash with Read Accelerator
  - Up to 16 KB of SRAM
  - 8-channel DMA engine
- Programmable analog
  - Two opamps with reconfigurable high-drive external and high-bandwidth internal drive and comparator modes and ADC input buffering capability. Opamps can operate in Deep Sleep low-power mode.
  - 12-bit 1-Msps SAR ADC with differential and single-ended modes, and channel sequencer with signal averaging
  - Single-slope 10-bit ADC function provided by a capacitance sensing block
  - Two current DACs (IDACs) for general-purpose or capacitive sensing applications on any pin
  - Two low-power comparators that operate in Deep Sleep low-power mode
- Programmable digital
  - Programmable logic blocks allowing Boolean operations to be performed on port inputs and outputs
- Low-power 1.71 V to 5.5 V operation
  - Deep Sleep mode with operational analog and 2.5 A digital system current
- Capacitive sensing
  - Capacitive sigma-delta (CSD) provides best-in-class signal-to-noise ratio (SNR) (> 5:1) and water tolerance
  - Infineon-supplied software component makes capacitive sensing design easy
  - Automatic hardware tuning (SmartSense)
- LCD drive capability
  - LCD segment drive capability on GPIOs
- Serial communication
  - Five independent run-time reconfigurable serial communication blocks (SCBs) with re-configurable I^2C, SPI, UART functionality, or LIN slave functionality
- Timing and pulse-width modulation
  - Eight 16-bit timer/counter/pulse-width modulator (TCPWM) blocks
  - Center-aligned, Edge, and Pseudo-random modes
  - Comparator-based triggering of Kill signals for motor drive and other high-reliability digital logic applications

Features

- Clock sources
  - 4 to 33 MHz external crystal oscillator (ECO)
  - PLL to generate 48-MHz frequency
  - 32-kHz watch crystal oscillator (WCO)
  - ±2% internal main oscillator (IMO)
  - 32-kHz internal low-power oscillator (ILO)
- True random number generator (TRNG)
  - TRNG generates truly random number for secure key generation for cryptography applications
- CAN block
  - CAN 2.0B block with support for time-triggered CAN (TTCAN)
- Temperature range
  - Grade-A: –40°C to +85°C
  - Grade-S: –40°C to +105°C
  - Grade-E: –40°C to +125°C
- Up to 54 programmable GPIO pins
  - 40-pin QFN, 64-pin QFN, and 64-pin TQFP packages
  - Any GPIO pin can be CAPSENSE™, analog, or digital
  - Drive modes, strengths, and slew rates are programmable
- PSoC™ Creator design environment
  - Integrated development environment (IDE) provides schematic design entry and build (with analog and digital automatic routing)

More information

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right PSoC™ device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article **How to design with PSoC™ 3, PSoC™ 4, and PSoC™ 5LP - KBA86521**. Following is an abbreviated list for PSoC™ 4:

- Overview: **PSoC™ portfolio**
- Product selectors: **PSoC™ 1**, **PSoC™ 3**, **PSoC™ 4**, **PSoC™ 5LP**
  In addition, PSoC™ Creator includes a device selection tool.
- Application notes: Infineon offers a large number of PSoC™ application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC™ 4 are:
  - **AN79953**: Getting started With PSoC™ 4
  - **AN88619**: PSoC™ 4 hardware design considerations
  - **AN86439**: Using PSoC™ 4 GPIO pins
  - **AN57821**: Mixed signal circuit board layout
  - **AN81623**: Digital design best practices
  - **AN73854**: Introduction to bootloaders
  - **AN89610**: Arm® Cortex® code optimization
  - **AN85951**: PSoC™ 4 and PSoC™ analog coprocessor CAPSENSE™ design guide
- Technical reference manual (TRM) is in two documents:
  - **Architecture TRM** details each PSoC™ 4 functional block.
  - **Registers TRM** describes each of the PSoC™ 4 registers.
- Development kits:
  - **CY8CKIT-041-41XX** PSoC™ 4100S CAPSENSE™ Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino™ compatible shields.
  - **CY8CKIT-149** PSoC™ 4100S Plus prototyping kit enables you to evaluate and develop with Infineon's fourth-generation, low-power CAPSENSE™ solution using the PSoC™ 4100S Plus devices.

The **MiniProg3** device provides an interface for flash programming and debug.

- **Software user guide**:
  - A step-by-step guide for using PSoC™ Creator. The software user guide shows you how the PSoC™ Creator build process works in detail, how to use source control with PSoC™ Creator, and much more.
- Component datasheets:
  - The flexibility of PSoC™ allows the creation of new peripherals (components) long after the device has gone into production. Component datasheets provide all the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.
- Online:
  - In addition to print documentation, the **Infineon community page** connects you with fellow PSoC™ users and experts in PSoC™ from around the world, 24 hours a day, 7 days a week.

PSoC™ Creator

PSoC™ Creator is a free Windows-based integrated design environment (IDE). It enables concurrent hardware and firmware design of PSoC™ 3, PSoC™ 4, and PSoC™ 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC™ Components; see the **list of component datasheets**. With PSoC™ Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC™ hardware, using the PSoC™ Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

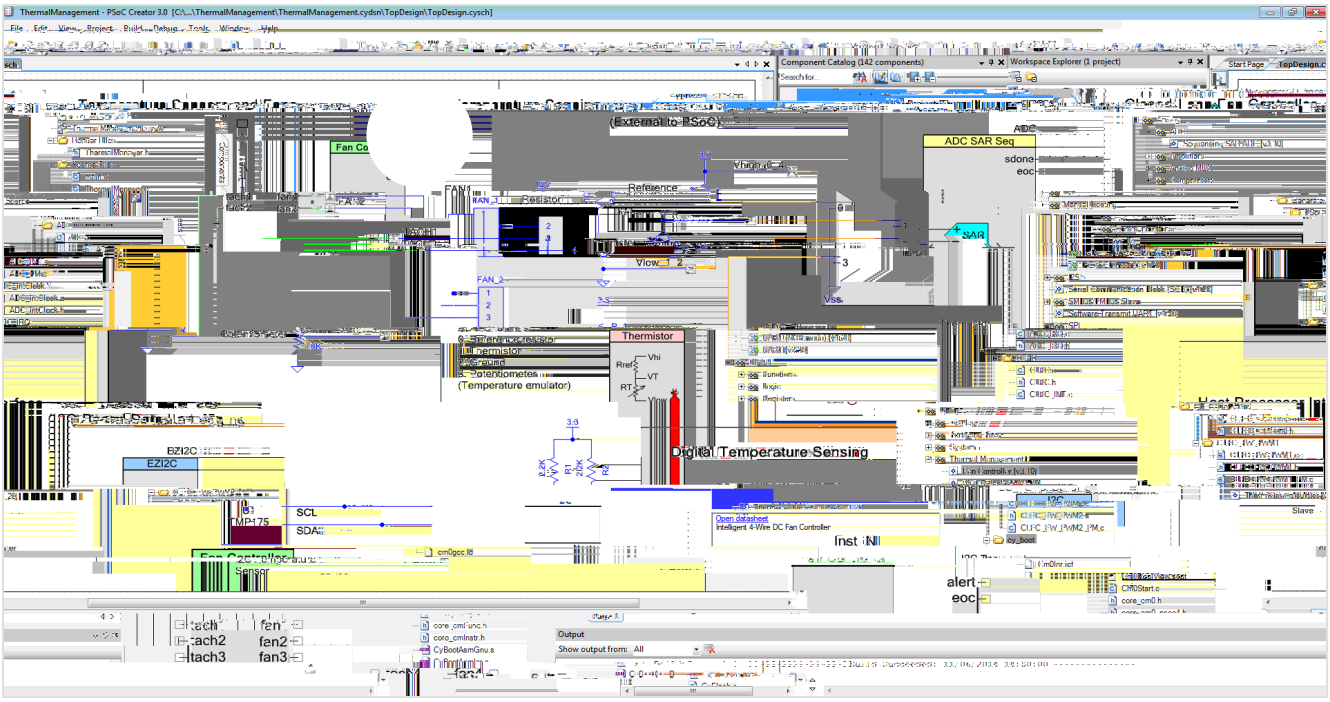


Figure 1 Multiple-sensor example project in PSoC™ Creator

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Block diagram

PSoC™ 4100S Plus devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The Arm® serial-wire debug (SWD) in

1 Functional definition

1.1 CPU and memory subsystem

1.1.1 CPU

The Cortex®-M0+ CPU in the PSoC™ 4100S Plus is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. Most instructions are 16 bits in length and the CPU executes a subset of the Thumb-2 instruction set. It includes a nested vectored interrupt controller (NVIC) block with eight interrupt inputs and also includes a Wakeup Interrupt Controller (WIC). The WIC can wake the processor from Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in Deep Sleep mode.

The CPU subsystem includes an 8-channel DMA engine and also includes a debug interface, the SWD interface, which is a 2-wire form of JTAG. The debug configuration used for PSoC™ 4100S Plus has four breakpoint (address) comparators and two watchpoint (data) comparators.

1.1.2 Flash

The PSoC™ 4100S Plus device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The low-power flash block is designed to deliver two wait-state (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average.

1.1.3 SRAM

16 KB of SRAM are provided with zero wait-state access at 48 MHz.

1.1.4 SROM

An 8-KB supervisory ROM that contains boot and configuration routines is provided.

1.2 System resources

1.2.1 Power system

The power system is described in detail in the section **“Power”** on page 20. It provides assurance that voltage levels are as required for each respective mode and either delays mode entry (for example, on power-on reset (POR)) until voltage levels are as required for proper functionality, or generates resets (for example, on brownout detection). PSoC™ 4100S Plus operates with a single external supply over the range of either 1.8 V ±5% (externally regulated) or 1.8 V to 5.5 V (internally regulated) and has three different power modes, transitions between which are managed by the power system. PSoC™ 4100S Plus provides Active, Sleep, and Deep Sleep low-power modes.

All subsystems are operational in Active mode. The CPU subsystem (CPU, flash, and SRAM) is clock-gated off in Sleep mode, while all peripherals and interrupts are active with instantaneous wake-up on a wake-up event. In Deep Sleep mode, the high-speed clock and associated circuitry is switched off; wake-up from this mode takes 35 µs. The opamps can remain operational in Deep Sleep mode.

1.2.2 Clock system

The PSoC™ 4100S Plus clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that there are no metastable conditions.

The clock system for the PSoC™ 4100S Plus consists of the IMO, ILO, a 32-kHz watch crystal oscillator (WCO), MHz ECO and PLL, and provision for an external clock. The WCO block allows locking the IMO to the 32-kHz oscillator.

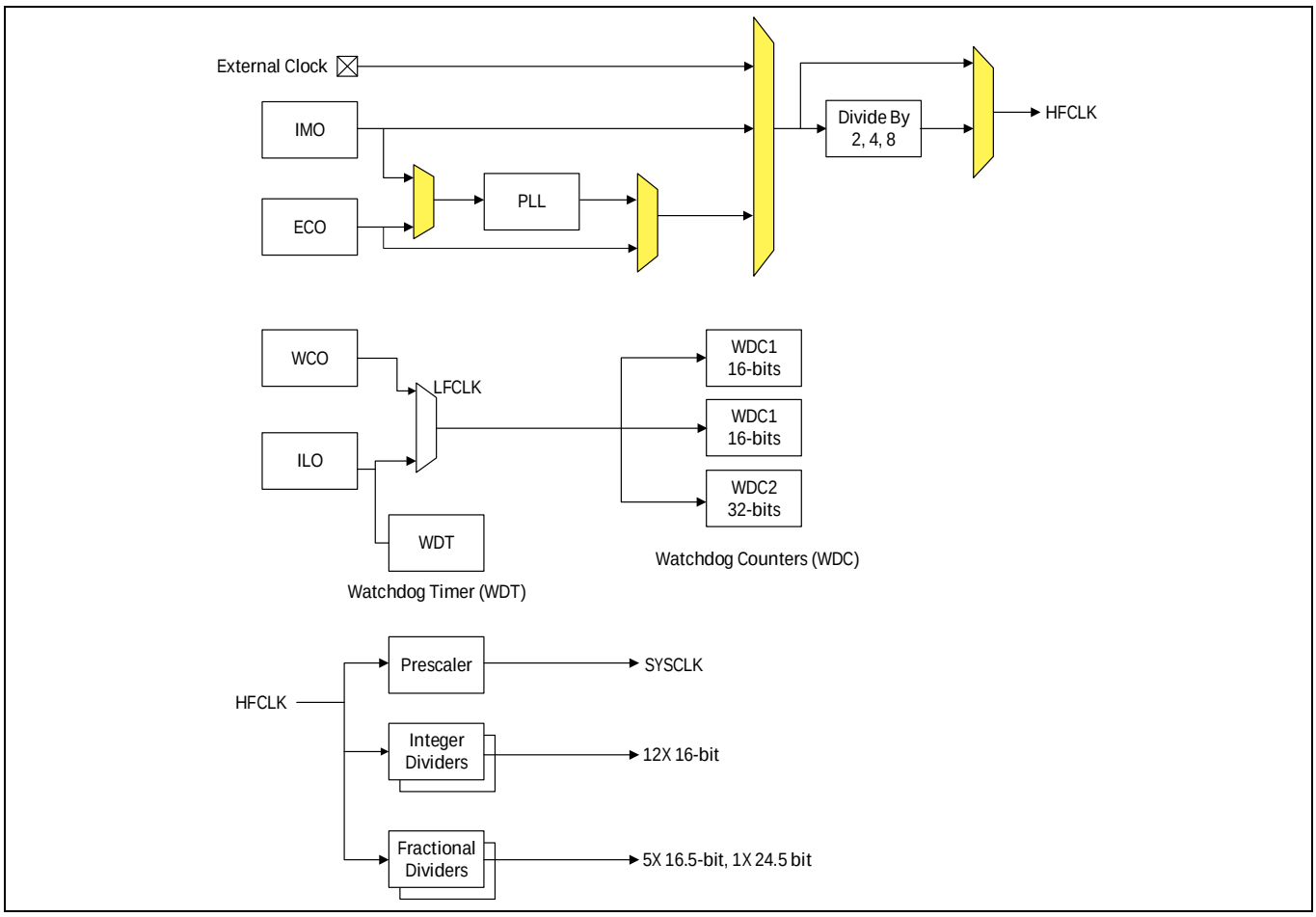


Figure 2 PSoC™ 4100S Plus MCU clocking architecture

The HFCLK signal can be divided down as shown to generate synchronous clocks for the Analog and Digital peripherals. There are 18 clock dividers for the PSoC™ 4100S Plus (six with fractional divide capability, twelve with integer divide only). The twelve 16-bit integer divide capability allows a lot of flexibility in generating fine-grained frequency. In addition, there are five 16-bit fractional dividers and one 24-bit fractional divider.

1.2.3 IMO clock source

The IMO is the primary source of internal clocking in the PSoC™ 4100S Plus. It is trimmed during testing to achieve the specified accuracy.The IMO default frequency is 24 MHz and it can be adjusted from 24 to 48 MHz in steps of 4 MHz. The IMO tolerance with Infineon-provided calibration settings is ±2% over the entire voltage and temperature range.

1.2.4 ILO clock source

The ILO is a very low power, nominally 40-kHz oscillator, which is primarily used to generate clocks for the watchdog timer (WDT) and peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Infineon provides a software component, which does the calibration.

1.2.5 WCO

The PSoC™ 4100S Plus clock subsystem also implements a low-frequency (32-kHz watch crystal) oscillator that can be used for precision timing applications.

1.2.6 ECO

The PSoC™ 4100S Plus also implements a 4 to 33 MHz crystal oscillator.

1.2.7 WDT

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the set timeout occurs. The watchdog reset is recorded in a Reset Cause register, which is firmware readable.

1.2.8 Reset

PSoC™ 4100S Plus can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset by asserting it active low. The XRES pin has an internal pull-up resistor that is always enabled.

1.3 Analog blocks

1.3.1 12-bit SAR ADC

The 12-bit, 1-Msps SAR ADC can operate at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. It is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) with zero switching overhead (that is, aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is not available in Deep Sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

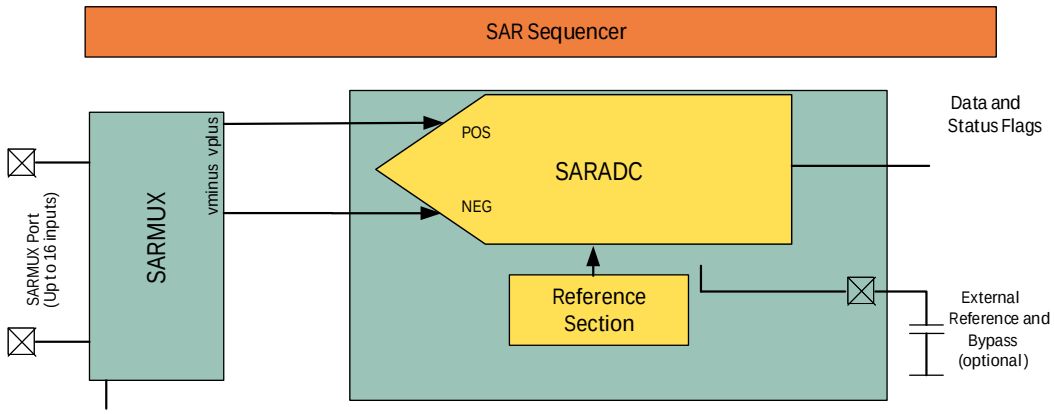


Figure 3 SAR ADC

1.3.2 Two opamps (continuous-time block; CTB)

PSoC™ 4100S Plus has two opamps with Comparator modes which allow most common analog functions to be performed on-chip eliminating external components; PGAs, voltage buffers, filters, trans-impedance amplifiers, and other functions can be realized, in some cases with external passives. saving power, cost, and space. The on-chip opamps are designed with enough bandwidth to drive the sample-and-hold circuit of the ADC without requiring external buffering.

1.3.3 Low-power comparators (LPC)

PSoC™ 4100S Plus has a pair of low-power comparators, which can also operate in Deep Sleep modes. This allows the analog system blocks to be disabled while retaining the ability to monitor external voltage levels during low-power modes. The comparator outputs are normally synchronized to avoid metastability unless operating in an asynchronous power mode where the system wake-up circuit is activated by a comparator switch event. The LPC outputs can be routed to pins.

1.3.4 Current DACs

PSoC™ 4100S Plus has two IDACs, which can drive any of the pins on the chip. These IDACs have programmable current ranges.

1.3.5 Analog multiplexed buses

PSoC™ 4100S Plus has two concentric independent buses that go around the periphery of the chip. These buses (called amux buses) are connected to firmware-programmable analog switches that allow the chip's internal resources (IDACs, comparator) to connect to any pin on the I/O ports.

1.4 Programmable digital blocks

1.4.1 Smart I/O block

The Smart I/O block is a fabric of switches and LUTs that allows Boolean functions to be performed in signals being routed to the pins of a GPIO port. The Smart I/O can perform logical operations on input pins to the chip and on signals going out as outputs.

1.5 Fixed function digital blocks

1.5.1 Timer/counter/PWM (TCPWM) block

The TCPWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register that is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals that are used as PWM duty cycle outputs. The block also provides true and

1.6 GPIO

PSoC™ 4100S Plus has up to 54 GPIOs. The GPIO block implements the following:

- Eight drive modes:
  - Analog input mode (input and output buffers disabled)
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addO

2 Pinouts

Table 1 40-pin QFN package pin list

Pin	Name
22	P0.0
23	P0.1
24	P0.2
25	P0.3
26	P0.4
27	P0.5
28	P0.6
29	P0.7
30	XRES
31	VCCD
32	VSSD
33	VDD
34	VSSA
35	P1.0
36	P1.1
37	P1.2
38	P1.3
39	P1.4
40	P1.7/VREF
1	P2.3
2	P2.4
3	P2.5
4	P2.6
5	P2.7
6	P6.0
7	P6.1
8	P6.2
9	VSSD
10	P3.0
11	P3.1
12	P3.2
13	P3.3
14	P3.4
15	P3.5
16	P3.6
17	P3.7
18	P4.0

Table 1 40-pin QFN package pin list *(continued)*

Pin	Name
19	P4.1
20	P4.2
21	P4.3

Table 2 64-pin QFN and 64-pin TQFP packages pin list

Pin	Name
39	P0.0
40	P0.1
41	P0.2
42	P0.3
43	P0.4
44	P0.5
45	P0.6
46	P0.7
47	XRES
48	VCCD
49	VSSD
50	VDDD
51	P5.0
52	P5.1
53	P5.2
54	P5.3
55	P5.5
56	VDDA
57	VSSA
58	P1.0
59	P1.1
60	P1.2
61	P1.3
62	P1.4
63	P1.5
64	P1.6
1	P1.7
2	P2.0
3	P2.1
4	P2.2
5	P2.3
6	P2.4
7	P2.5
8	P2.6

2.1 Alternate pin functions

Each port pin has can be assigned to one of multiple functions; it can, for example, be an analog I/O, a digital peripheral function, an LCD pin, or a CAPSENSE™ pin. The pin assignments are shown in the following table.

Table 3 Pin assignments

Analog	Smart I/O	ACT #0	ACT #1	ACT #3	DS #2	DS #3
lpcomp.in_p[0]			tcpwm.tr_in[0]	scb[2].uart_cts:0	s124,(98063.7n:9(A)-2.7(s2136)-69.3(t)-4.30].spi_sele)4.00	

P1.7	ctb0_oa1+ sar_ext_vref0 sar_ext_vref1	SmartIo[2].io[7]	tcpwm.line_-compl[7]:1				scb[2].spi_clk:1
P2.0	sarmux[0]	SmartIo[0].io[0]	tcpwm.line[4]:0	csd.comp	tcpwm.tr_in[4]	scb[1].i2c_scl:1	scb[1].spi_mosi:2
P2.1	sarmux[1]	SmartIo[0].io[1]	tcpwm.line_compl[4]:0		tcpwm.tr_in[5]	scb[1].i2c_sda:1	scb[1].spi_miso:2

P3.6		SmartIo[1].io[6]	tcpwm.line[3]:0			scb[4].spi_select3	scb[1].spi_select3:0
P3.7		SmartIo[1].io[7]	tcpwm.line_compl[3]:0			lpcomp.comp[1]:1	scb[2].spi_miso:1
P4.0	csd.vref_ext			scb[0].uart_rx:0	can.can_rx:1	scb[0].i2c_scl:1	scb[0].spi_mosi:0
P4.1	csd.cshield			scb[0].uart_tx:0	can.can_tx:1	scb[0].i2c_sda:1	scb[0].spi_miso:0
P4.2	csd.cmod			scb[0].uart_cts:0	can.can_tx_enb_n:1	lpcomp.comp[0]:1	scb[0].spi_clk:0

3 Power

The following power system diagram shows the set of power supply pins as implemented for the PSoC™ 4100S Plus. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the VDDA input.

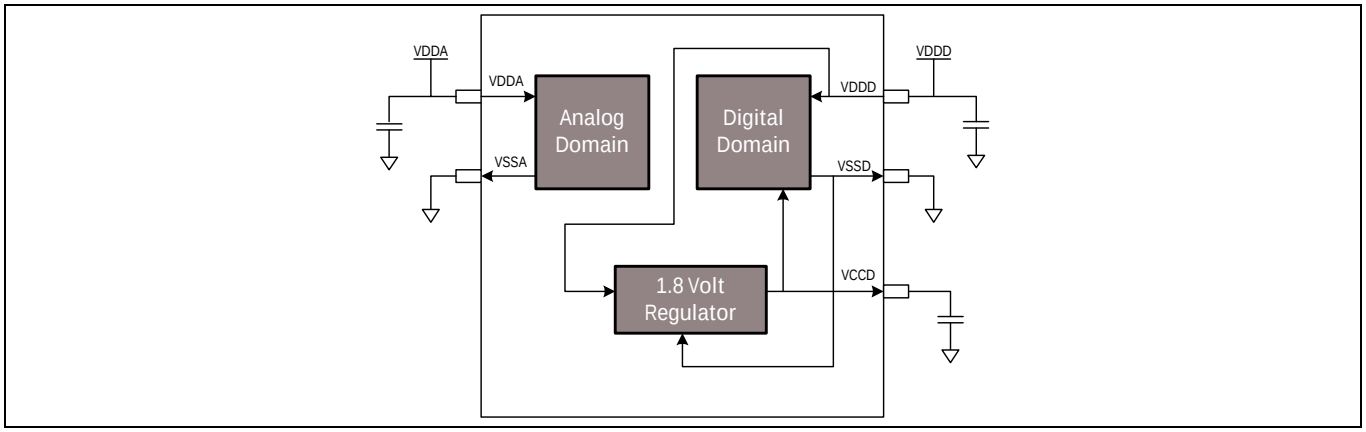


Figure 4 Power supply connections

There are two distinct modes of operation. In Mode 1, the supply voltage range is 1.8 V to 5.5 V (unregulated externally; internal regulator operational). In Mode 2, the supply range is1.8 V ±5% (externally regulated; 1.71 to 1.89, internal regulator bypassed).

3.1 Mode 1: 1.8 V to 5.5 V external supply

In this mode, PSoC™ 4100S Plus is powered by an external power supply that can be anywhere in the range of 1.8 to 5.5 V. This range is also designed for battery-powered operation. For example, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC™ 4100S Plus supplies the internal logic and its output is connected to the VCCD pin. The VCCD pin must be bypassed to ground via an external capacitor (0.1 µF; X5R ceramic or better) and must not be connected to anything else.

3.2 Mode 2: 1.8 V ± 5% external supply

In this mode, PSoC™ 4100S Plus is powered by an external power supply that must be within the range of 1.71 to 1.89 V; note that this range needs to include the power supply ripple too. In this mode, the VDD and VCCD pins are shorted together and bypassed.

Bypass capacitors must be used from VDDD to ground. The typical practice for systems in this frequency range is to use a capacitor in the 1-µF range, in parallel with a smaller capacitor (0.1 µF, for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing. On some packages, VDDD and VDDA pins are shorted inside the package and brought out as a generic VDD pin. In that case, only 0.1-µF and 1-µF decoupling capacitors are required on the VDD pin.

An example of a bypass scheme is shown in the following diagram.

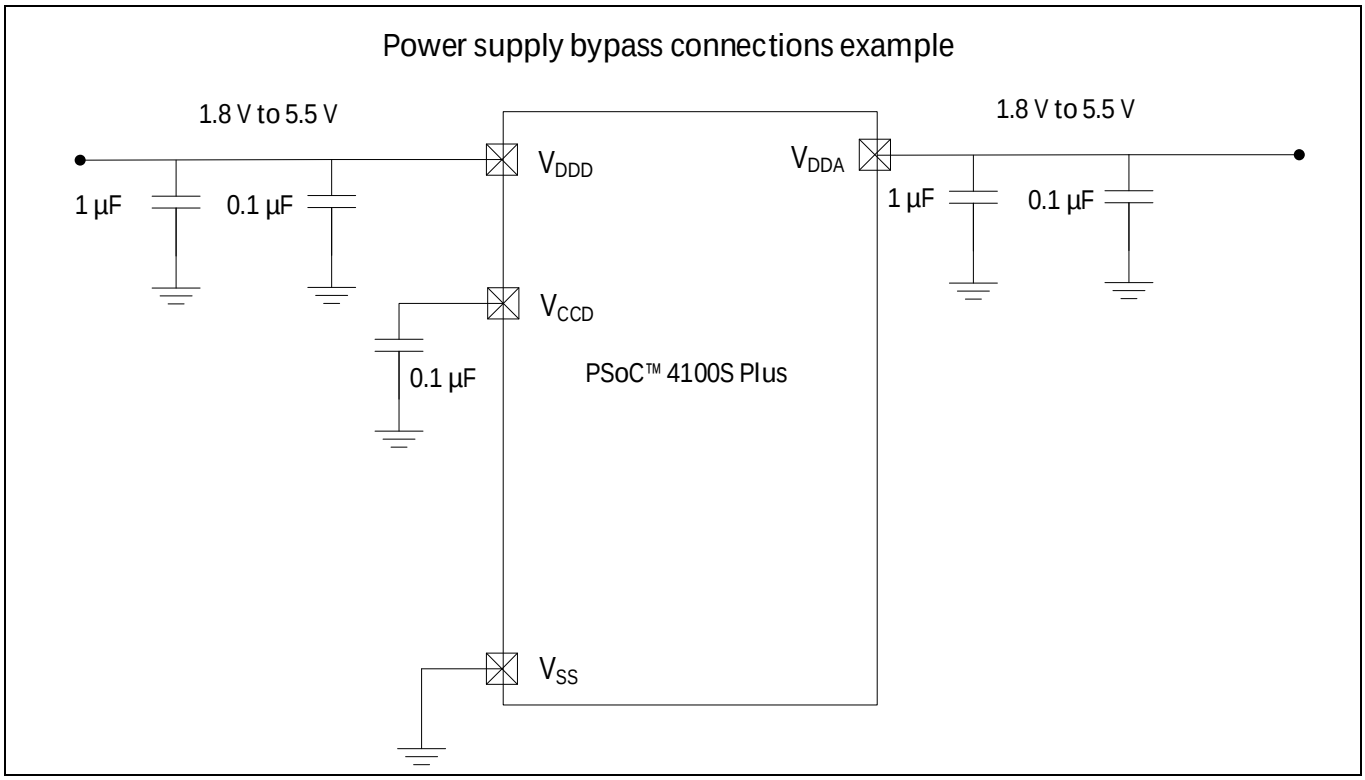


Figure 5 External supply range from 1.8 V to 5.5 V with internal regulator active

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4 Absolute maximum ratings[1]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID1	V_{DDD_ABS}	Digital supply relative to V_{SS}	–0.5	–	6	V	–
SID2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SS}	–0.5	–	1.95		–
SID3	V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DD} + 0.5		–
SID4	I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
SID5	$I_{GPIO_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
BID45	ESD_CDM	Electrostatic discharge charged device model	500	–	–		–
BID46	LU	Pin current for latch-up	–140	–	140	mA	–

Note
1. Usage above the absolute maximum conditions listed in **Table 4** may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

4.2 Device-level specifications

All specifications are valid for –40°C ≤ TA ≤ 85°C for Grade-A devices, –40°C ≤ TA ≤ 105°C for Grade-S devices, and –40°C ≤ TA ≤ 125°C for Grade-E devices. Specifications are valid for 1.71 V to 5.5 V, except where noted.

Table 5 DC specifications

Typical values measured at V_{DD} = 3.3 V and 25°C.

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID53	V_{DD}	Power supply input voltage	1.8	–	5.5	V	Internally regulated supply
SID255	V_{DD}	Power supply input voltage (V_{CCD} = V_{DDD} = V_{DDA})	1.71	–	1.89		Internally unregulated supply
SID54	V_{CCD}	Output voltage (for core logic)	–	1.8	–		–
SID55	C_{EFC}	External regulator voltage bypass	–	0.1	–	µF	X5R ceramic or better
SID56	C_{EXC}	Power supply bypass capacitor	–	1	–		X5R ceramic or better
Active mode, V_{DD} = 1.8 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V and 25°C.							
SID10	I_{DD5}	Execute from flash; CPU at 6 MHz	–	1.8	2.7	mA	Max is at 125°C and 5.5 V
SID16	I_{DD8}	Execute from flash; CPU at 24 MHz	–	3.0	5		Max is at 125°C and 5.5 V
SID19	I_{DD11}	Execute from flash; CPU at 48 MHz	–	5.4	7.6		Max is at 125°C and 5.5 V
Sleep mode, VDDD = 1.8 V to 5.5 V (Regulator on)							
SID22	I_{DD17}	I^2C wakeup WDT, and Comparators on	–	1.1	2.2	mA	6 MHz. Max is at 125°C and 5.5 V
SID25	I_{DD20}	I^2C wakeup, WDT, and Comparators on	–	1.5	2.5		12 MHz. Max is at 125°C and 5.5 V
Sleep mode, V_{DDD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID28	I_{DD23}	I^2C wakeup, WDT, and Comparators on	–	1.1	1.8	mA	6 MHz. Max is at 125°C and 1.89 V.
SID28A	I_{DD23A}	I^2C wakeup, WDT, and Comparators on	–	1.5	2.1		12 MHz. Max is at 125°C and 1.89 V.
Deep Sleep mode, V_{DD} = 1.8 V to 3.6 V (Regulator on)							
SID30	I_{DD25}	I^2C wakaR2 and WDT on	–	2.5	40	µA	T = –40°C to 60°C
SID31	I_{DD26}	I^2C wakaR2 and WDT on	–	2.5	350		Max is at 3.6 V and 125°C
Deep Sleep mode, V_{DD} = 3.6 V to 5.5 V (Regulator on)							
SID33	I_{DD28}	I^2C wakaR2 and WDT on	–	2.5	40	µA	T = –40°C to 60°C
SID34	I_{DD29}	I^2C wakaR2 and WDT on	–	2.5	350		Max is at 5.5 V and 125°C
Deep Sleep mode, V_{DD} = V_{CCD} = 1.71 V to 1.89 V (Regulator bypassed)							
SID36	I_{DD31}	I^2C wakaR2 and WDT on	–	2.5	60	µA	T = –40°C to 60°C
SID37	I_{DD32}	I^2C wakeand WDT on	–	2.5	400		Max is at 125°C and 1.89 V
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	2	5	mA	–

Table 6 AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID48	F_{CPU}	CPU frequency	DC	–	48	MHz	1.71 V_{DD} 5.5
SID49	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	–
SID50	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–		–

4.2.1 GPIO

Table 7 GPIO DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID57	V_{IH}[2]	Input voltage high threshold	0.7 V_{DDD}	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	0.3 V_{DDD}		CMOS Input
SID241	V_{IH}[2]	LVTTL input, V_{DDD} < 2.7 V	0.7 V_{DDD}	–	–		–
SID242	V_{IL}	LVTTL input, V_{DDD} < 2.7 V	–	–	0.3 V_{DDD}		–
SID243	V_{IH}[2]	LVTTL input, V_{DDD} 2.7 V	2.0	–	–		–
SID244	V_{IL}	LVTTL input, V_{DDD} 2.7 V	–	–	0.8		–
SID59	V_{OH}	Output voltage high level	V_{DDD} – 0.6	–	–		I_{OH} = 4 mA at 3 V V_{DDD}
SID60	V_{OH}	Output voltage high level	V_{DDD} – 0.5	–	–		I_{OH} = 1 mA at 1.8 V V_{DDD}
SID61	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 4 mA at 1.8 V V_{DDD}
SID62	V_{OL}	Output voltage low level	–	–	0.6		I_{OL} = 10 mA at 3 V V_{DDD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4		I_{OL} = 3 mA at 3 V V_{DDD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DDD} = 3.0 V
SID66	C_{IN}	Input capacitance	–	–	7	pF	–
SID67[3]	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	V_{DDD} 2.7 V
SID68[3]	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–		V_{DD} < 4.5 V
SID68A[3]	$V_{HYSCMOS5V5}$	Input hysteresis CMOS	200	–	–		V_{DD} > 4.5 V
SID69[3]	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	A	–
SID69A[3]	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	–

Notes
2. V_{IH} must not exceed V_{DDD} + 0.2 V.
3. Guaranteed by characterization.

Table 8 GPIO AC specifications
(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time in fast strong mode	2	–	12	ns	3.3 V V_{DDD}, Cload = 25 pF
SID71	T_{FALLF}	Fall time in fast strong mode	2	–	12		3.3 V V_{DDD}, Cload = 25 pF
SID72	T_{RISES}	Rise time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID73	T_{FALLS}	Fall time in slow strong mode	10	–	60	–	3.3 V V_{DDD}, Cload = 25 pF
SID74	$F_{GPIOUT1}$	GPIO F_{OUT}; 3.3 V V_{DDD} 5.5 V Fast strong mode	–	–	33	MHz	90/10%, 25 pF load, 60/40 duty cycle
SID75	$F_{GPIOUT2}$	GPIO F_{OUT}; 1.71 V V_{DDD} 3.3 V Fast strong mode	–	–	16.7		90/10%, 25 pF load, 60/40 duty cycle
SID76	$F_{GPIOUT3}$	GPIO F_{OUT}; 3.3 V V_{DDD} 5.5 V Slow strong mode	–	–	7		90/10%, 25 pF load, 60/40 duty cycle
SID245	$F_{GPIOUT4}$	GPIO F_{OUT}; 1.71 V V_{DDD} 3.3 V Slow strong mode.	–	–	3.5		90/10%, 25 pF load, 60/40 duty cycle
SID246	F_{GPIOIN}	GPIO input operating frequency; 1.71 V V_{DDD} 5.5 V					

4.2.2 XRES

Table 9 XRES DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID77	V_{IH}	Input voltage high threshold	0.7 × V_{DDD}	–	–	V	CMOS Input
SID78	V_{IL}	Input voltage low threshold	–	–	0.3 V_{DDD}		
SID79	R_{PULLUP}	Pull-up resistor	–	60	–	kΩ	–
SID80	C_{IN}	Input capacitance	–	–	7	pF	–
SID81[4]	$V_{HYSXRES}$	Input voltage hysteresis	–	100	–	mV	Typical hysteresis is 200 mV for V_{DD} > 4.5 V
SID82	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–

Table 10 XRES AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID83[4]	$T_{RESETWIDTH}$	Reset pulse width	1	–	–	µs	–
BID194[4]	$T_{RESETWAKE}$	Wake-up time from reset release	–	–	2.7	ms	–

Note
4. Guaranteed by characterization.

4.3 Analog peripherals

4.3.1 CTBm opamp

Table 11 CTBm opamp specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
	I_{DD}	Opamp block current, External load					
SID269	I_{DD_HI}	power = hi	–	1100	1850	µA	–
SID270	I_{DD_MED}	powe1 Tccccccmed		–	550	950	–
SID271	I_{DD_LOW}	powecccccIo		–	150	350	–
	G_{BW}	Load = 20 pF, 0.1 mA V_{DDA}cc5.5(2.7)-201.4(V)]TJET1 g279.72 554.54 273 28.5 ref44.7 514.04 54.96 40.5 refBT10.98 0 0 V					
							$_{DDA}$ – 0.5 V
SID276	$I_{OUT_MAX_MID}$	powercccmid	10	–	–		Output 5 V to V_{DDA} – 0.5 V
SID277	$I_{OUT_MAX_LO}$	powecccclo	–	5	–		Output 5 V to V_{DDA} – 0.5 V
	I_{OUT}	V_{DDA} = 1.71 V, 500 mV from rail					
SID278	$I_{OUT_MAX_HI}$	power = hi	4	–	–	mA	Output 5 V to V_{DDA} – 0.5 V
SID279	$I_{OUT_MAX_MID}$	powercccmid	4	–	–		Output 5 V to V_{DDA} – 0.5 V
SID280	$I_{OUT_MAX_LO}$	powercc5.5(Io)-7877.5(–)-3382.1(2)-3611(–)]TJET1 g457.68 205.04 95.04 28.5 refBT10.98 0 0 10 V					$_{DDA}$ – 0.5 V
	I_{DD_Int}	Opamp block current Internal Load					
SID269_I	$I_{DD_HI_Int}$	power = hi	–	1500	1700	µA	–

Table 11 CTBm opamp specifications *(continued)*

Spec ID#	Parameter	Description					
		General opamp specs for both internal and external modes					
SID281	V_{IN}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2	V	–
SID282	V_{CM}	Charge-pump on, V_{DDA} = 2.7 V	–0.05	–	V_{DDA} – 0.2		–
	V_{OUT}	V_{DDA} = 2.7 V					
SID283	V_{OUT_1}	power = hi, Iload = 10 mA	0.5	–	V_{DDA} – 0.5	V	–
SID284	V_{OUT_2}	power = hi, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID285	V_{OUT_3}	power = med, Iload = 1 mA	0.2	–	V_{DDA} – 0.2		–
SID286	V_{OUT_4}	power = lo, Iload = 0.1 mA	0.2	–	V_{DDA} – 0.2		–
SID288	V_{OS_TR}	Offset voltage, trimmed	–1.0	0.5	1.0	mV	High mode, input 0 V to V_{DDA} – 0.2 V
SID288A	V_{OS_TR}	Offset voltage, trimmed	–	1.4	–		Medium mode, input 0 V to V_{DDA} – 0.2 V
SID288B	V_{OS_TR}	Offset voltage, trimmed	–	2	–		Low mode, input 0 V to V_{DDA} – 0.2 V
SID290	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–10	3	10	µV/°C	High mode
SID290A	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	10	–	µV/°C	Medium mode
SID290B	$V_{OS_DR_TR}$	Offset voltage drift, trimmed	–	10	–		Low mode
SID291	CMRR	DC	70	80	–	dB	Input is 0 V to V_{DDA} – 0.2 V, Output is 0.2 V to V_{DDA} – 0.2 V
SID292	PSRR	At 1 kHz, 10-mV ripple	70	85	–		V_{DDD} = 3.6 V, high-power mode, input is 0.2 V to V_{DDA} – 0.2 V
	Noise						
SID294	VN2	Input-referred, 1 kHz, power = Hi	–	72	–	nV/ rtHz	3
SID295	VN3	Input-referred, 10 kHz, power = Hi	–	28	–		Input and output are at 0.2 V to V_{DDA} – 0.2 V
SID296	VN4	Input-referred, 100 kHz, power = Hi	–	15	–		Input and output are at 0.2 V to V_{DDA} – 0.2 V

SID297	C_{LOAD}	Stable up to max. load. Performance specs at 50 pF.	–	–	125	pF	–
SID298	SLEW_RATE	Cload = 50 pF, Power = High, V_{DDA} = 2.7 V	6	–	–	V/µs	–
SID299	T_OP_WAKE	From disable to enable, no external RC dominating	–	–	25	µs	–
SID299A	OL_GAIN	Open Loop Gain	–	90	–	dB	–
	COMP_ MODE	Comparator mode; 50 mV drive, T_{rise} = T_{fall} (approx.)					
SID300	TPD1	Response time; power = hi	–	150	–	ns	Input is 0.2 V to V_{DDA} – 0.2 V
SID301	TPD2	Response time; power = med	–	500	–		Input is 0.2 V to V_{DDA} – 0.2 V
SID302	TPD3	Response time; power = lo	–	2500	–		Input is 0.2 V to V_{DDA} – 0.2 V
SID303	VHYST_OP	Hysteresis	–	10	–	mV	–
SID304	WUP_CTB	Wake-up time from Enabled to Usable	–	–	25	µs	–
	Deep Sleep Mode	Mode 2 is lowest current range. Mode 1 has higher GBW.					

4.3.2 Comparator

Table 12 Comparator DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID84	$V_{OFFSET1}$	Input offset voltage, Factory trim	–	–	±10	mV	–
SID85	$V_{OFFSET2}$	Input offset voltage, Custom trim	–	–	±4		–
SID86	V_{HYST}	Hysteresis when enabled	–	10	35		–
SID87	V_{ICM1}	Input common mode voltage in normal mode	0	–	V_{DDD} – 0.1	V	Modes 1 and 2
SID247	V_{ICM2}	Input common mode voltage in low power mode	0	–	V_{DDD}		–
SID247A	V_{ICM3}	Input common mode voltage in ultra low power mode	0	–	V_{DDD} – 1.15		$V_{DDD} \geq 2.2$ V at –40°C
SID88	C_{MRR}	Common mode					

4.3.3 Temperature sensor

Table 14 Temperature sensor specifications

4.3.4 SAR ADC

SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	–1.5	–	1.7	LSB	V_{REF} = 1.71 to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1.5	–	1.7	LSB	V_{REF} = 1 to V_{DD}
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	–1	–	2.2	LSB	V_{REF} = 1 to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6, 1 Msps	–1	–	2	LSB	V_{REF} = 1.71 to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	–1	–	2.2	LSB	V_{REF} = 1 to V_{DD}
SID113	A_THD	Total harmonic distortion	–	–	–65	dB	Fin = 10 kHz
SID261	FSARINTREF	SAR operating speed without external reference bypass	–	–	100	ksps	12-bit resolution

4.3.5 CSD and IDAC

Table 16 CSD and IDAC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
	VDD_RIPPLE	Max allowed ripple on power supply, DC to 10 MHz	–	–	±50	mV	V_{DD} > 2 V (with ripple), 25°C T_A, Sensitivity = 0.1 pF
SYS.PER#16	VDD_RIPPLE_1.8	Max allowed ripple on power supply, DC to 10 MHz	–	–	±25	mV	V_{DD} > 1.75V (with ripple), 25°C T_A, Parasitic Capacitance (C_P) < 20 pF, Sensitivity ≥ 0.4 pF
SID.CSD.BLK	ICSD	Maximum block current	–	–	4000	µA	Maximum block current for both IDACs in dynamic (switching) mode including comparators, buffer, and reference generator
SID.CSD#15	V_{REF}	Voltage reference for CSD and Comparator	0.6	1.2	V_{DDA} – 0.6	V	V

SID.CSD#17	IDAC2IDD	IDAC2 (7-bits) block current	–	–	1750	µA	–
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	1.8 V ± 5% or 1.8 V to 5.5 V
SID308A	VCOMPIDAC	Voltage compliance range of IDAC	0.6	–	V_{DDA} – 0.6	V	V_{DDA} – 0.06 or 4.4, whichever is lower
SID309	IDAC1DNL	DNL	–1	–	1	LSB	–

Table 16 CSD and IDAC specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID315D	IDAC2CRT22	Output current of IDAC2 (7 bits) in medium range, 2X mode	69	–	82	µA	LSB = 600 nA typ
SID315E	IDAC2CRT32	Output current of IDAC2 (7 bits) in high range, 2X mode	540	–	660	µA	LSB = 4.8 µA typ
SID315F	IDAC3CRT13	Output current of IDAC in 8-bit mode in low range	8	–	10.5	µA	LSB = 37.5 nA typ
SID315G	IDAC3CRT23	Output current of IDAC in 8-bit mode in medium range	69	–	82	µA	LSB = 300 nA typ
SID315H	IDAC3CRT33	Output current of IDAC in 8-bit mode in high range	540	–	660	µA	LSB = 2.4 µA typ
SID320	IDACOFFSET	All zeroes input	–	–	1	LSB	Polarity set by Source or Sink. Offset is 2 LSBs for 37.5 nA/LSB mode
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	–
SID322	IDACMISMATCH1	Mismatch between IDAC1 and IDAC2 in Low mode	–	–	9.2	LSB	LSB = 37.5 nA typ
SID322A	IDACMISMATCH2	Mismatch between IDAC1 and IDAC2 in Medium mode	–	–	5.6	LSB	LSB = 300 nA typ
SID322B	IDACMISMATCH3	Mismatch between IDAC1 and IDAC2 in High mode	–	–	6.8	LSB	LSB = 2.4 µA typ
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	5	µs	Full-scale transition. No external load
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	5	µs	Full-scale transition. No external load
SID325	CMOD	External modulator capacitor.	–	2.2	–	nF	5-V rating, X7R or NP0 cap

4.3.6 10-bit CAPSENSE™ ADC

Table 17 10-bit CAPSENSE™ ADC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SIDA94	A_RES	Resolution	–	–	10	bits	Auto-zeroing is required every millisecond
SIDA95	A_CHNLS_S	Number of channels - single ended	–	–	16		Defined by AMUX Bus
SIDA97	A-MONO	Monotonicity	–	–	–	Yes	–
SIDA98	A_GAINERR	Gain error	–	–	±3	%	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA99	A_OFFSET	Input offset voltage	–	–	±18	mV	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA101	A_VINS	Input voltage range - single ended	V_{SSA}	–	V_{DDA}	V	–
SIDA103	A_INRES	Input resistance	–	2.2	–	KΩ	–
SIDA104	A_INCAP	Input capacitance	–	20	–	pF	–
SIDA106	A_PSRR	Power supply rejection ratio	–	60	–	dB	In V_{REF} (2.4 V) mode with V_{DDA} bypass capacitance of 10 µF
SIDA107	A_TACQ	Sample acquisition time	–	1	–	µs	–
SIDA108	A_CONV8	Conversion time for 8-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	21.3	µs	Does not include acquisition time. Equivalent to 44.8 ksps including acquisition time.
SIDA108A	A_CONV10	Conversion time for 10-bit resolution at conversion rate = Fhclk/(2^(N+2)). Clock frequency = 48 MHz.	–	–	85.3	µs	Does not include acquisition time. Equivalent to 11.6 ksps including acquisition time.
SIDA109	A_SND	Signal-to-noise and Distortion ratio (SINAD)	–	61	–	dB	With 10-Hz input sine wave, external 2.4-V reference, V_{REF} (2.4 V) mode
SIDA110	A_BW	Input bandwidth without aliasing	–	–	22.4	KHz	8-bit resolution
SIDA111	A_INL	Integral Non Linearity. 1 ksps	–	–	2	LSB	V_{REF} = 2.4 V or greater
SIDA112	A_DNL	Differential Non Linearity. 1 ksps	–	–	1		–

4.4 Digital peripherals

4.4.1 Timer counter pulse-width modulator (TCPWM)

Table 18 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	–	–	155		All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	–	–	650		All modes (TCPWM)
SID.TCPWM.3	$TCPWM_{FREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$TPWM_{ENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events[5]
SID.TCPWM.5	$TPWM_{EXT}$	Output trigger pulse widths	2/Fc	–	–		Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	TC_{RES}	Resolution of counter	1/Fc	–	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–		Minimum pulse width of PWM Output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–		Minimum pulse width between Quadrature phase inputs

4.4.2 I²C

Table 19 Fixed I²C DC specifications[5]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	50	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	310		–
SID152	I_{I2C4}	I²C enabled in Deep Sleep mode	–	1	–		–

Table 20 Fixed I²C AC specifications[5]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Msps	–

Note
5. Guaranteed by characterization.

4.4.3 SPI

Table 21 SPI DC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps	–	–	560		–
SID165	ISPI3	Block current consumption at 8 Mbps	–	–	600		–

Table 22 SPI AC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI Operating frequency (Master; 6X Oversampling)	–	–	8	MHz	–
Fixed SPI Master mode AC specifications							
SID167	TDMO	MOSI Valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge
Fixed SPI Slave mode AC specifications							
SID170	TDMI	MOSI Valid before Sclock Capturing edge	40	–	–	ns	–
SID171	TDSO	MISO Valid after Sclock driving edge	–	–	42 + (3 × Tcpu)		$T_{CPU} = 1/F_{CPU}$
SID171A	TDSO_EXT	MISO Valid after Sclock driving edge in Ext. Clk mode	–	–	48		–
SID172	THSO	Previous MISO data hold time	0	–	–		–
SID172A	TSSELSSCK	SSEL Valid to first SCK Valid edge	–	–	100	ns	–

4.4.4 UART

Table 23 UART DC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	55	µA	–
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312	µA	–

Table 24 UART AC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

4.4.5 LCD Direct Drive

Table 25 LCD Direct Drive DC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID154	I_{LCDLOW}	Operating current in low power mode	–	5	–	µA	16 4 small segment disp. at 50 Hz
SID155	C_{LCDCAP}	LCD capacitance per segment/common driver	–	500	5000	pF	–
SID156	LCD_{OFFSET}	Long-term segment offset	–	20	–	mV	–
SID157	I_{LCDOP1}	LCD system operating current Vbias = 5 V	–	2	–	mA	32 4 segments at 50 Hz, 25°C
SID158	I_{LCDOP2}	LCD system operating current Vbias = 3.3 V	–	2	–		32 4 segments at 50 Hz, 25°C

Table 26 LCD Direct Drive AC specifications[6]

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID159	F_{LCD}	LCD frame rate	10	50	150	Hz	–

Note
6. Guaranteed by characterization.

4.5 Memory

4.5.1 Flash

Table 27 Flash DC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}						

4.6 System resources

4.6.1 Power-on reset (POR)

Table 29 Power-on reset (PRES)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/conditions
SID.CLK#6	SR_POWER	Power supply slew rate	1[8]	–	67	V/ms	On power-up and power-down
SID185[9]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[9]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

4.6.2 Brown-out detect (BOD)

Table 30 Brown-out detect (BOD) for V_{CCD}

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190[9]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[9]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

4.6.3 SWD interface

Table 31 SWD interface specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID213	F_SWDCLK1	3.3 V V_{DD} 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	1.71 V V_{DD} 3.3 V	–	–	7		SWDCLK ≤ 1/3 CPU clock frequency
SID215[9]	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	–
SID216[9]	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–		–
SID217[9]	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.5 × T		–
SID217A[9]	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–		–

Notes
8. If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp (1.5 V > V_{DDD} > 1.0 V for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I2C bus could occur during voltage ramp in this case.
9. Guaranteed by characterization.

4.6.4 Internal main oscillator

Table 32 IMO DC specifications

(Guaranteed by design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO1}	IMO operating current at 48 MHz	–	–	250	µA	–
SID219	I_{IMO2}	IMO operating current at 24 MHz	–	–	180	µA	–

Table 33 IMO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID223	$F_{IMOTOL1}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2	%	–40°C ≤ TA ≤ 105°C
SID223A	$F_{IMOTOL1A}$	Frequency variation at 24, 32, and 48 MHz (trimmed)	–	–	±2.5	%	–40°C ≤ TA ≤ 125°C
SID333	IMO_{WCO}	All IMO settings	–	–	±0.25	%	IMO variation in WCO-locked DPLL mode
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	–
SID228	$T_{JITRMSIMO2}$	RMS jitter at 24 MHz	–	145	–	ps	–

4.6.5 Internal low-speed oscillator

Table 34 ILO DC specifications

(Guaranteed by Design)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO1}	ILO operating current	–	0.3	1.05	µA	–

Table 35 ILO AC specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234[10]	$T_{STARTILO1}$	ILO startup time	–	–	2	ms	–
SID236[10]	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	–
SID237	$F_{ILOTRIM1}$	ILO frequency range	20	40	80	kHz	–

4.6.6 Watch crystal oscillator (WCO)

Table 36 WCO specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID398	FWCO	Crystal frequency	–	32.768	–	kHz	–
SID399	FTOL	Frequency tolerance	–	50	250	ppm	

4.6.7 External clock

4.6.9 System clock

Table 40 Block specs

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID262[12]	$T_{CLKSWITCH}$	System clock source switching time	3	–	4	Periods	–

4.6.10 Smart I/O

Table 41 Smart I/O pass-through time (Delay in Bypass Mode)

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID252	PRG_BYPASS	Max delay added by Smart I/O in bypass mode	–	–	1.6	ns	–

4.6.11 CAN

Table 42 CAN specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID420	IDD_CAN	Block current consumption	–	–	200	µA	–
SID421	CAN_bits	CAN Bit rate	–	–	1	Mbps	Min 8-MHz clock

Note
12.Guaranteed by characterization.

5 Ordering information

Table 43 lists the marketing part numbers (MPNs) for the PSoC™ 4100S Plus devices[13].

Table 43 Ordering information

MPN	Features															Packages			Operating temperaure		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CAPSENSE™	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	WCO	ECO	Smart IOs	CAN	GPIO	40-QFN	64-WQFN	64-TQFP	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4126AZA-S455	24	64	8	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4146AZA-S245	48	64	8	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4146AZA-S255	48	64	8	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4146AZA-S265	48	64	8	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4146AZA-S275	48	64	8	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4146AZA-S455	48	64	8	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4127AZA-S445	24	128	16	-	2	-	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4127AZA-S455	24	128	16	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S245	48	128	16	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S255	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S265	48	128	16	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S275	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S285	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	X	-	-
CY8C4147AZA-S295	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	X	-	-
CY8C4147AZA-S445	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S455	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	X	-	-
CY8C4147AZA-S465	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	X	-	-
CY8C4147AZA-S475	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	X	-	-
CY8C4126AZS-S455	24	64	8	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4146AZS-S245	48	64	8	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4146AZS-S255	48	64	8	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4146AZS-S265	48	64	8	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4146AZS-S275	48	64	8	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4146AZS-S455	48	64	8	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4127AZS-S445	24	128	16	-	2	-	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-

Note
13. Contact **Infineon Support** for the availability of Grade-E devices.
14. Alternate fab available.

Table 43 Ordering information *(continued)*

MPN	Features															Packages			Operating temperaure		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CAPSENSE™	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	WCO	ECO	Smart IOs	CAN	GPIO	40-QFN	64-WQFN	64-TQFP	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4127AZS-S455	24	128	16	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S245	48	128	16	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S255	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S265[14]	48	128	16	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S275	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S285[14]	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	X	-
CY8C4147AZS-S295	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	X	-
CY8C4147AZS-S445	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S455	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	X	-
CY8C4147AZS-S465	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	X	-
CY8C4147AZS-S475	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	X	-
CY8C4126LQA-S453	24	64	8	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4146LQA-S243	48	64	8	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4146LQA-S253	48	64	8	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4146LQA-S263	48	64	8	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4146LQA-S273	48	64	8	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4146LQA-S453	48	64	8	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4127LQA-S443	24	128	16	-	2	-	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4127LQA-S453	24	128	16	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S243	48	128	16	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S253	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S263	48	128	16	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S273	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S283	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	X	-	-
CY8C4147LQA-S293	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	X	-	-
CY8C4147LQA-S443	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S453	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	X	-	-
CY8C4147LQA-S463	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	X	-	-
CY8C4147LQA-S473	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	X	-	-
CY8C4126LQS-S453	24	64	8	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-

Note
13. Contact **Infineon Support** for the availability of Grade-E devices.
14. Alternate fab available.

Table 43 Ordering information *(continued)*

MPN	Features															Packages			Operating temperaure		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CAPSENSE™	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	WCO	ECO	Smart IOs	CAN	GPIO	40-QFN	64-WQFN	64-TQFP	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4146LQS-S243	48	64	8	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4146LQS-S253	48	64	8	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4146LQS-S263	48	64	8	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4146LQS-S273	48	64	8	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4146LQS-S453	48	64	8	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4127LQS-S443	24	128	16	-	2	-	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4127LQS-S453	24	128	16	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S243	48	128	16	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S253	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S263	48	128	16	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S273	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S283[14]	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	X	-
CY8C4147LQS-S293	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	X	-
CY8C4147LQS-S443	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S453	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	X	-
CY8C4147LQS-S463	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	X	-
CY8C4147LQS-S473	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	X	-
CY8C4126LQE-S453	24	64	8	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4146LQE-S243	48	64	8	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4146LQE-S253	48	64	8	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4146LQE-S263	48	64	8	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4146LQE-S273	48	64	8	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4146LQE-S453	48	64	8	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4127LQE-S443	24	128	16	-	2	-	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4127LQE-S453	24	128	16	-	2	X	X	806 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S243	48	128	16	-	-	-	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S253	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S263	48	128	16	-	-	X	-	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S273	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S283[14]	48	128	16	-	-	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	-	X

Note
13. Contact **Infineon Support** for the availability of Grade-E devices.
14. Alternate fab available.

Table 43 Ordering information *(continued)*

MPN	Features															Packages			Operating temperaure		
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm)	CAPSENSE™	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	WCO	ECO	Smart IOs	CAN	GPIO	40-QFN	64-WQFN	64-TQFP	-40 to +85C	-40 to +105C	-40 to +125C
CY8C4147LQE-S293	48	128	16	-	-	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	-	X
CY8C4147LQE-S443[14]	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S453	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	-	34	X	-	-	-	-	X
CY8C4147LQE-S463	48	128	16	-	2	-	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	-	X
CY8C4147LQE-S473	48	128	16	-	2	X	X	1000 Ksps	2	8	4	X	X	24	1	34	X	-	-	-	-	X
CY8C4126AZE-S455	24	64	8	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4146AZE-S245	48	64	8	-	-	-	-	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4146AZE-S255	48	64	8	-	-	-	X	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4146AZE-S265	48	64	8	-	-	X	-	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4146AZE-S275	48	64	8	-	-	X	X	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4146AZE-S455	48	64	8	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4127AZE-S445	24	128	16	-	2	-	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4127AZE-S455	24	128	16	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4147AZE-S245	48	128	16	-	-	-	-	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4147AZE-S255	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4147AZE-S265	48	128	16	-	-	X		1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4147AZE-S275	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	-	-	54	-	-	X	-	-	X
CY8C4147AZE-S285	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	-	X
CY8C4147AZE-S295[14]	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	-	X
CY8C4147AZE-S445	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4147AZE-S455	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	-	X	-	-	X
CY8C4147AZE-S465	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	-	X
CY8C4147AZE-S475	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	-	X	-	-	X
CY8C4126LQA-S455	24	64	8	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4146LQA-S245	48	64	8	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4146LQA-S255	48	64	8	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4146LQA-S265	48	64	8	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4146LQA-S275	48	64	8	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4146LQA-S455	48	64	8	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-
CY8C4127LQA-S445	24	128	16	-	2	-	X	806 Ksps	2	8	5	X	X	24	-	54	-	X	-	X	-	-

Note
13. Contact **Infineon Support** for the availability of Grade-E devices.
14. Alternate fab available.

Automotive PSoC™ 4: PSoC™ 4100S Plus
Based on Arm® Cortex®-M0+ CPU

Ordering information

)-w 1T1 (8 20 0Y8C42227LQA-S455 Q 7L-24 48 8 25 128 12 244 16S2 8-- YAX 0Q. 02 6 60 4 1 05 2XX 64 1 5 8 8 2 0)-3 w26 Y2 C5 01 X 6 - 0 J0 6 T-]4)10 -6) w 3X 0- S0 0- 04 (1 (3 . 9 8 6 2 - 4)

Table 43 Ordering information *(continued)*

MPN	Features															Packages			Operating temperaure	
	Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Opamp (CTBm.3534 -769-6.92c-.47CA Tw9(.0															
CY8C4146LQE-S245	48	64	8	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4146LQE-S255	48	64	8	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4146LQE-S265	48	64	8	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4146LQE-S275	48	64	8	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4146LQE-S455	48	64	8	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4127LQE-S445	24	128	16	-	2	-	X	806 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4127LQE-S455	24	128	16	-	2	X	X	806 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S245	48	128	16	-	-	-	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S255	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S265	48	128	16	-	-	X	-	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S275	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S285	48	128	16	-	-	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	X	-	-	-	X
CY8C4147LQE-S295	48	128	16	-	-	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	X	-	-	-	X
CY8C4147LQE-S445	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S455	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	-	54	-	X	-	-	-	X
CY8C4147LQE-S465	48	128	16	-	2	-	X	1000 Ksps	2	8	5	X	X	24	1	54	-	X	-	-	-	X
CY8C4147LQE-S475	48	128	16	-	2	X	X	1000 Ksps	2	8	5	X	X	24	1	54	-	X	-	-	-	X

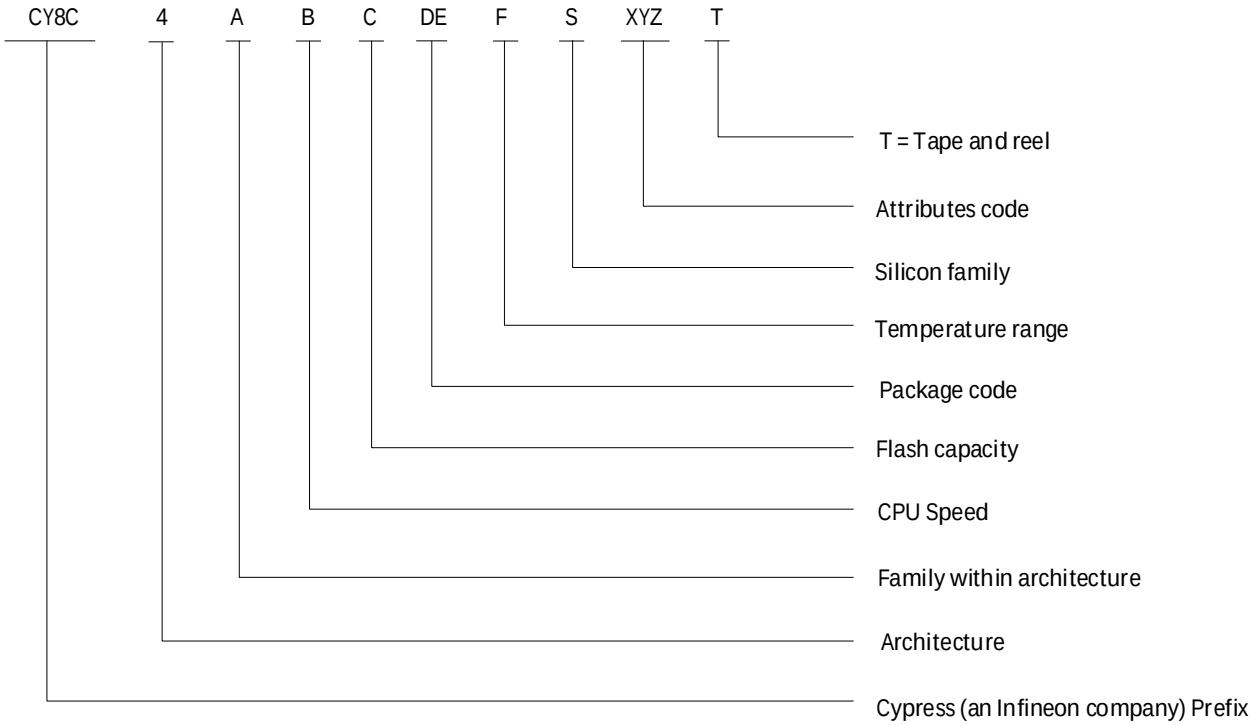
Ordering information

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress (an Infineon company) prefix		
4	Architecture	4	PSoC™ 4
A	Family	1	4100 family
B	CPU speed	2	24 MHz
		4	48 MHz
C	Flash capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package code	AZ	TQFP (0.5-mm pitch)
		LQ	QFN
F	Temperature range	A	Automotive (AEC-Q100: –40°C to +85°C)
		S	Automotive (AEC-Q100: –40°C to +105°C)
		E	Automotive (AEC-Q100: –40°C to +125°C)
S	Silicon family	S	PSoC™ 4 S-Series
		M	PSoC™ 4 M-Series
		L	PSoC™ 4 L-Series
		BL	PSoC™ 4 Bluetooth® LE-Series
XYZ	Attributes code	000–999	Code of feature set in the specific family

Ordering information

The following is an example of a part number:



Example
4: PSoC™ 4
1: 4100 family
4: 48 MHz
6: 64 KB
AZ: TQFP
A, S, E: Automotive

6 Packaging

The PSoC™ 4100S Plus will be offered in 40-pin QFN, 64-pin QFN, and 64-pin TQFP packages. **Table 44** provides the package dimensions

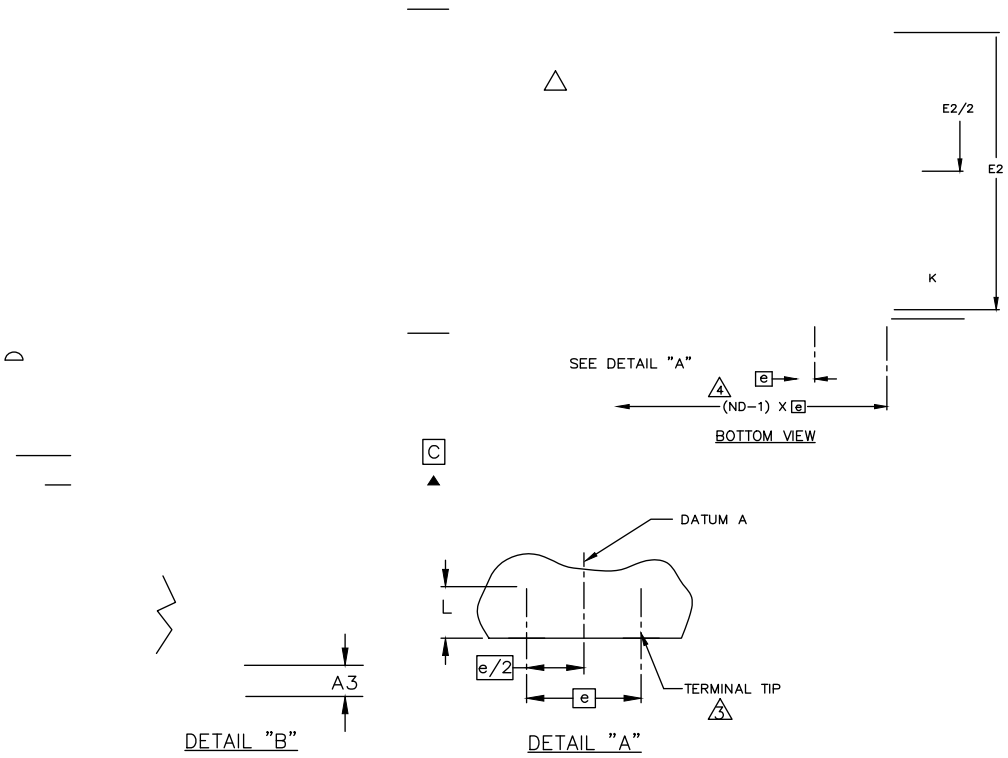
6.1 Package diagrams

51-85051 *D

Figure 6 64-pin TQFP (10 × 10 × 1.4 mm) package outline, 51-85051

002-25105 *A

Figure 7 40-pin QFN ((6 × 6 × 0.6 mm) 4.6 × 4.6 mm E-Pad (Sawn)) package outline, 002-25105



002-31760 **

Figure 8 64-pin QFN (9 × 9 × 0.9 mm) 7.70 × 7.70 mm E-Pad (Sawn)) package outline, 002-31760

7 Acronyms

Table 48 Acronyms used in this document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an Arm® data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
Arm®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	Dhrystone million instructions per second

Acronyms

FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC™ pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	

PLD	programmable logic device, see also PAL
PLL	
PMDD	

)p)]TJET1

Table 48 Acronyms used in this document *(continued)*

Acronym	Description
USB	Universal Serial Bus
USBIO	USB input/output, PSoC™ pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

Revision history

Document revision	Date	Description of changes
*O	2023-01-20	Post to external web.
*P	2023-05-02	Updated **Table 1** in **Pinouts**. Updated **Table 44** in **Packaging**. Removed spec 002-29721 ** in **Package diagrams**. Removed 48-pin QFN throughout the document.

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