TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M4F single

General description

Features

Dual CPU subsystem

Integrated memories

Crypto engine

I/O

Regulators

Programmable analog

Smart I/O™

Debug interface

Compatible with industry-standard tools

Packages

Certification

Table of contents

General description 1
Features 1
Table of contents 4
1 Features list 5

2 Blocks and functionality 7
Block diagram 7

28 Packaging 139
29 Appendix 146

30 Acronyms 148
31 Errata 150
Revision history 159

1 Features list

Table 1-1 CYT2B7 feature list for all packages

Features	Packages				
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP

Motor Control Input

Security

Flash Security (program/work read protection)

Flash Chip erase enable

eSHE/HSM

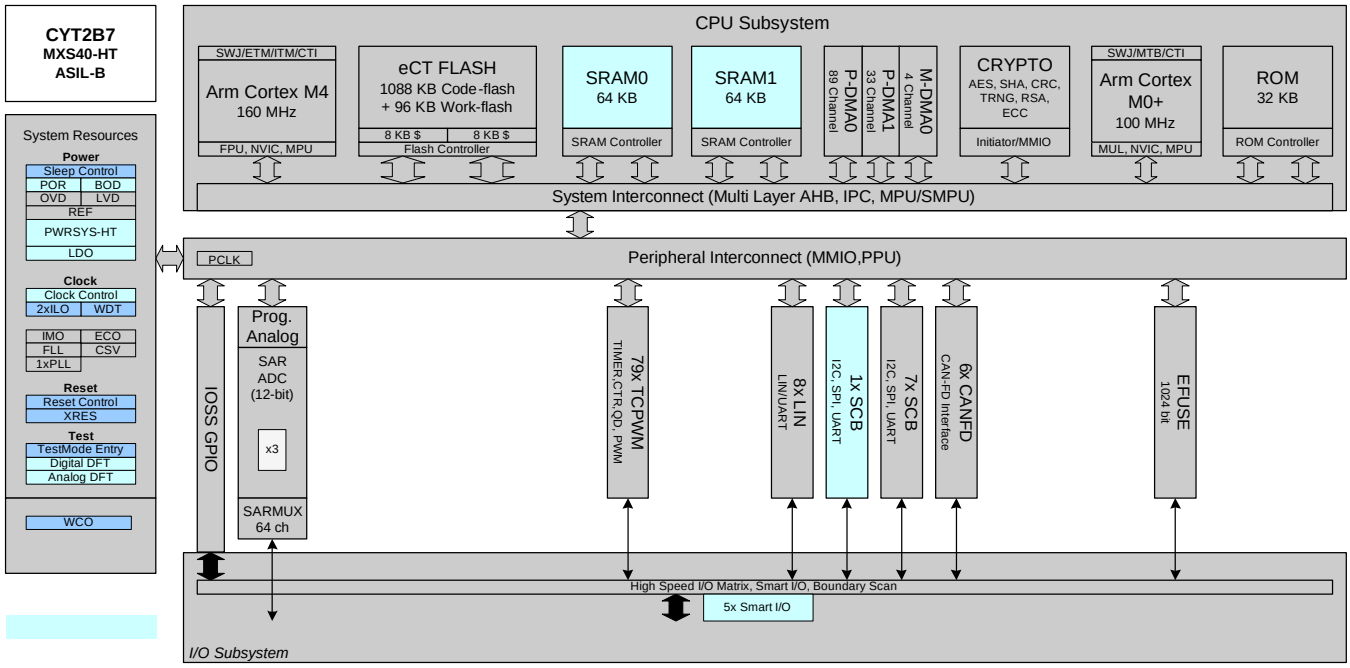
System

DMA Controller

1.1 Communication peripheral instance list

2 Blocks and functionality

Block diagram



Block diagram

3.2 System resources

3.2.1 Power system

3.2.3.3 IMO clock source

3.2.3.4 ILO clock source

3.2.3.5 PLL and FLL

3.2.3.6 Clock supervisor (CSV)

3.2.3.7 EXT_CLK

3.2.3.8 ECO

3.2.3.9 WCO

3.2.4 Reset

3.2.5 Watchdog timers

3.2.6 Power modes

3.3.3 12-bit SAR ADC

Table 1-1

3.3.4 Timer/counter/PWM block (TCPWM)

3.3.5 Serial communication blocks (SCB)

3.3.5.10 I^2C interface

3.3.5.11 *UART interface*

3.3.5.12 SPI interface

3.3.6 CAN FD

Notes

3.3.7 Local interconnect network (LIN)

3.3.8 One-time-programmable (OTP) eFuse

3.3.9 Event generator

3.3.10 Trigger multiplexer

3.4 I/Os

Table 3-1

3.4.1 Port nomenclature

3.4.2 Smart I/O

4 CYT2B7 address map

Figure 4-1

5 Flash base address map

Table 5-1 Table 5-6

Table 5-1 Code-flash Address Mapping in Single Bank Mode

Code-flash Size (KB)	Large Sectors (LS)	Small Sectors (SS)	Large Sector Base Address	Small Sector Base Address

Table 5-2 Work-flash Address Mapping in Single Bank Mode

Work-flash Size (KB)	Large Sectors	Small Sectors	Large Sector Base Address	Small Sector Base Address

Table 5-3 Code-flash Address Mapping in Dual Bank Mode (Mapping A)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address

Table 5-4 Code-flash Address Mapping in Dual Bank Mode (Mapping B)

Code-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address

Table 5-5 Work-flash Address Mapping in Dual Bank Mode (Mapping A)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address

Table 5-6 Work-flash Address Mapping in Dual Bank Mode (Mapping B)

Work-flash Size (KB)	First Half LS	First Half SS	Second Half LS	Second Half SS	First Half LS Base Address	First Half SS Base Address	Second Half LS Base Address	Second Half SS Base Address

6 Peripheral I/O map

Table 6-1 CYT2B7 peripheral I/O map

Section	Description	Base Address	Instances	Instance Size	Group	Slave

Note

7 CYT2B7 clock diagram

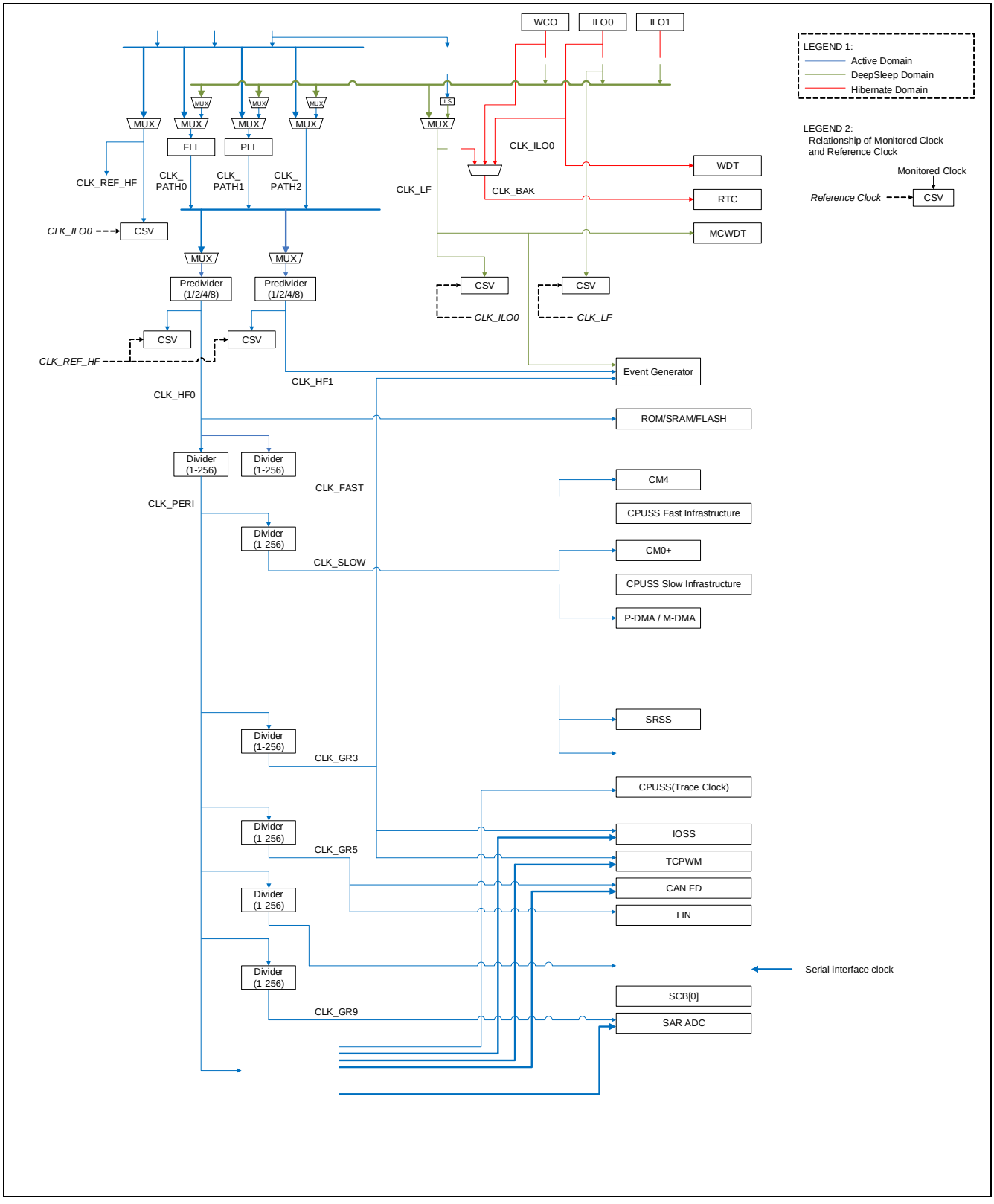


Figure 7-1 CYT2B7 clock diagram

8 CYT2B7 CPU start-up sequence

2. CM0+ executes ROM boot (@0x0000 0004)

3. CM0+ executes flash boot (from Supervisory flash @0x1700 2000)

9 Pin assignment

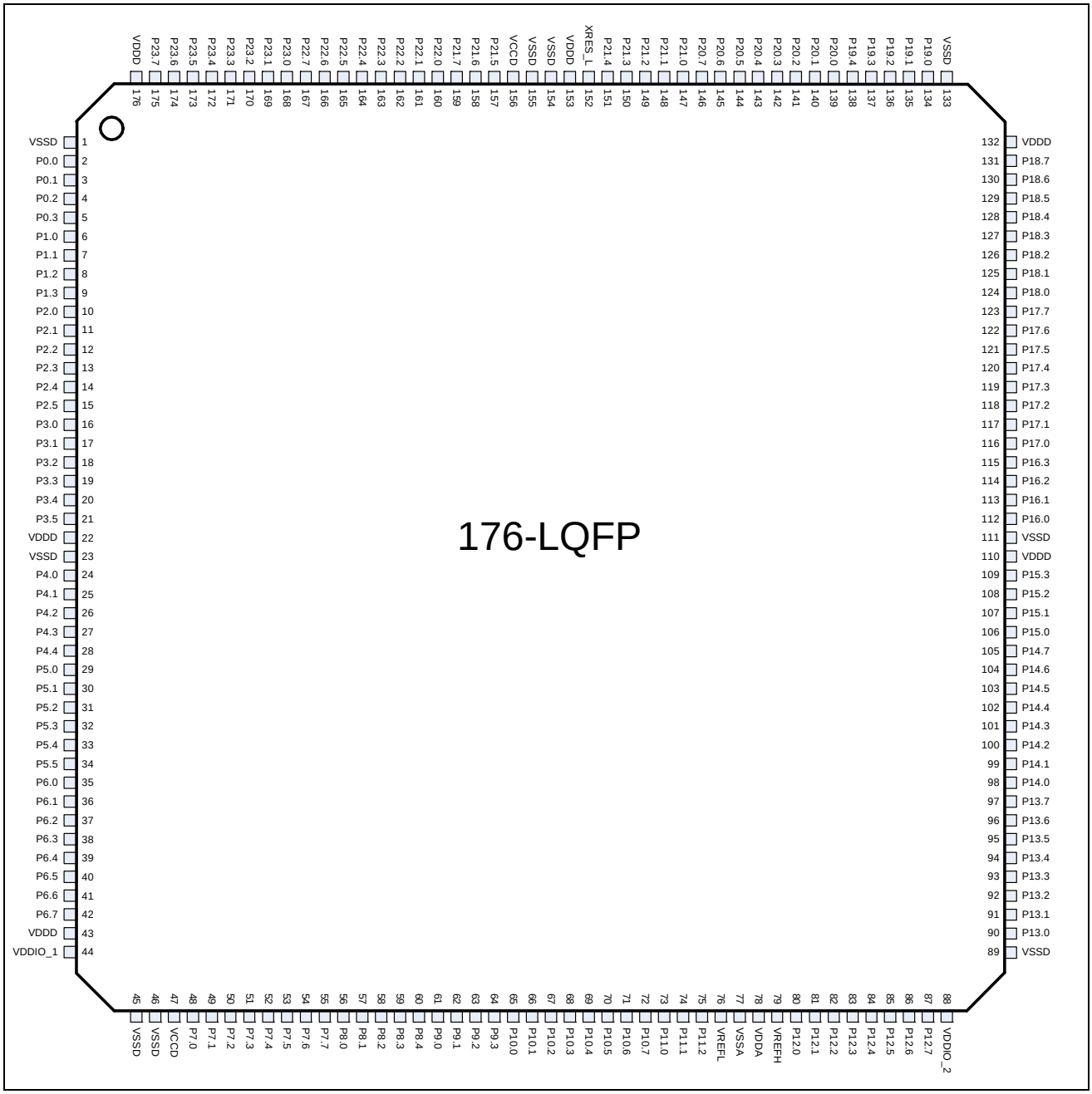


Figure 9-1 176-LQFP pin assignment

Figure 9-2 176-LQFP pin assignment with alternate functions

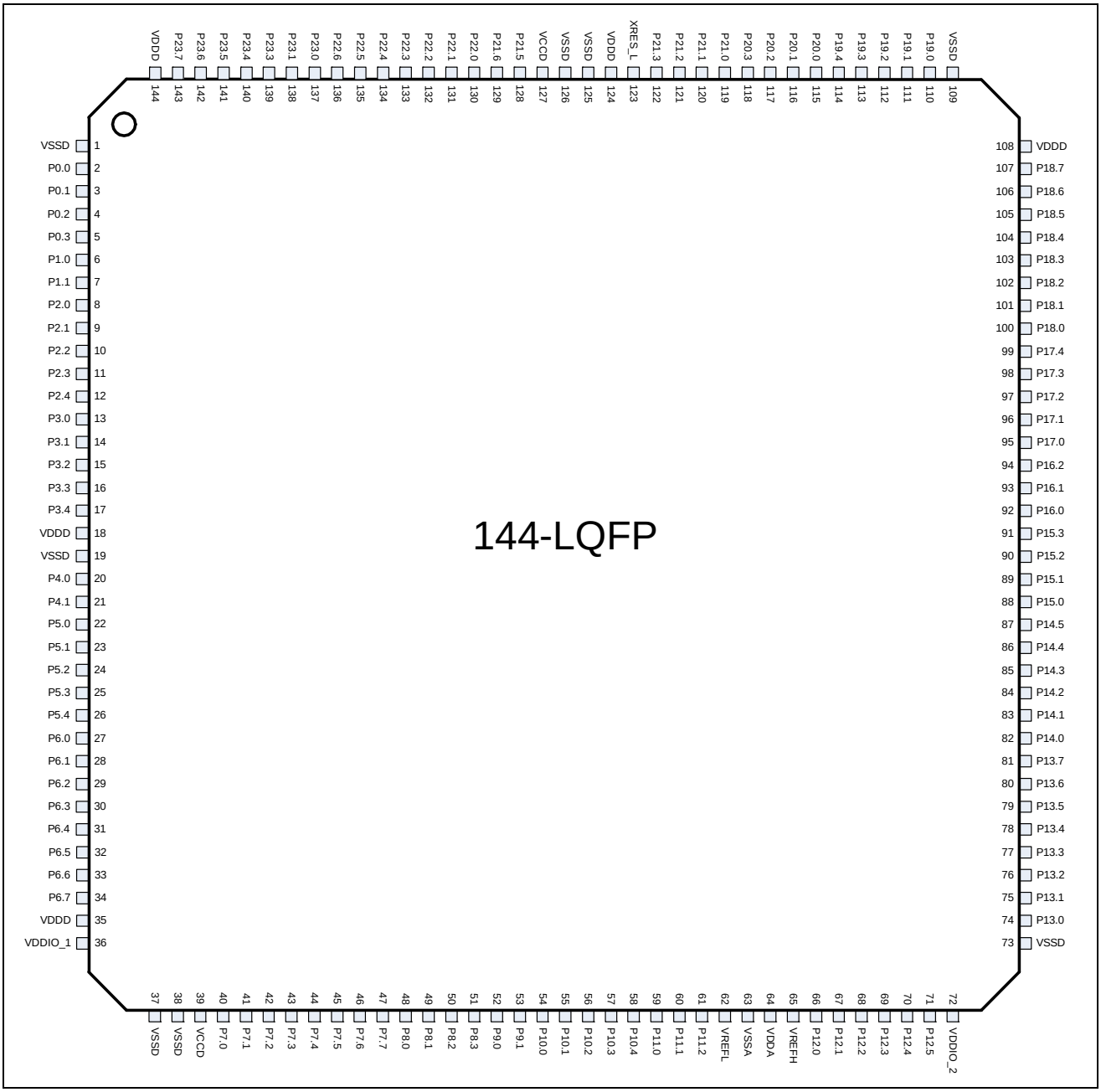


Figure 9-3 144-LQFP pin assignment

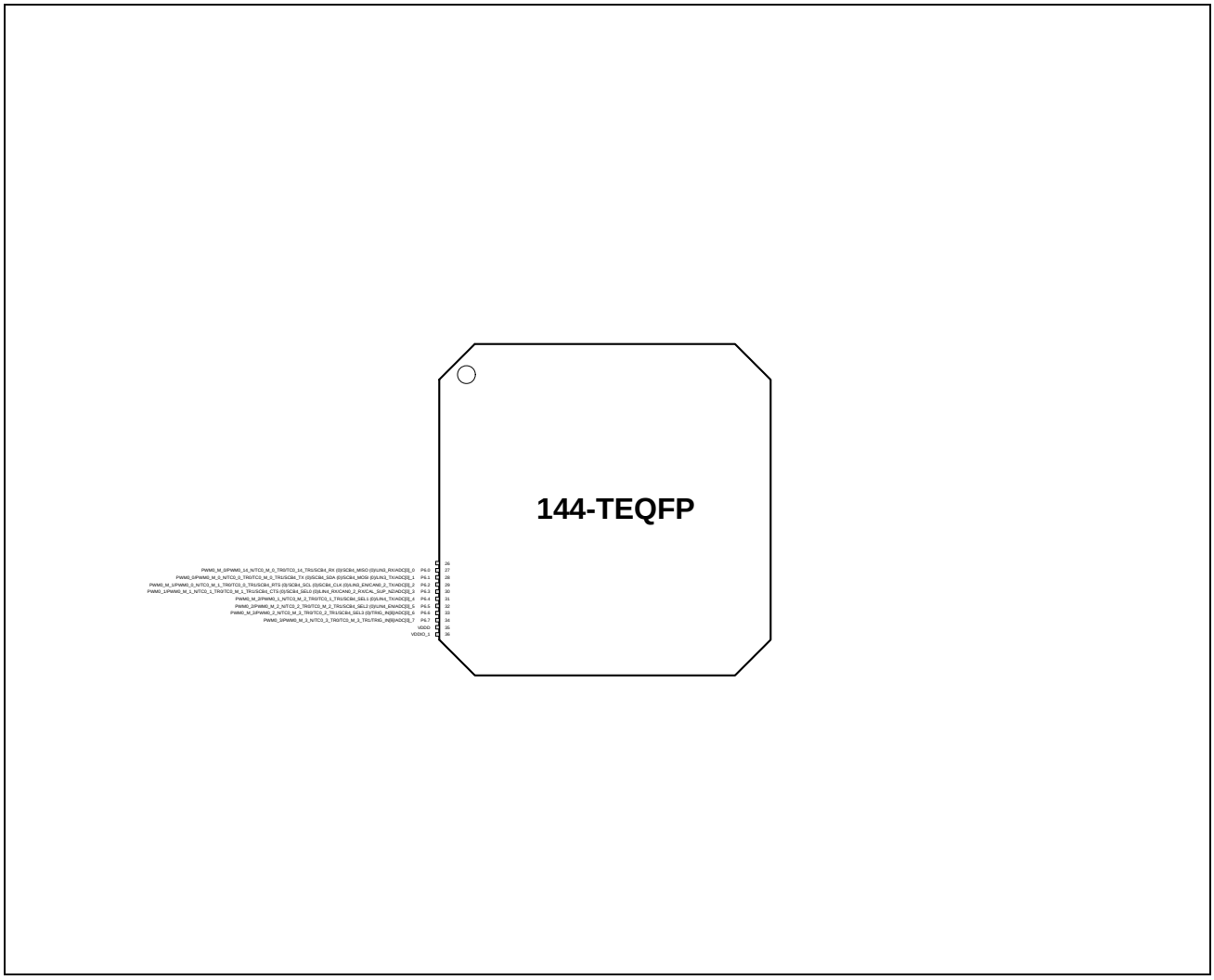


Figure 9-4 144-LQFP pin assignment with alternate functions

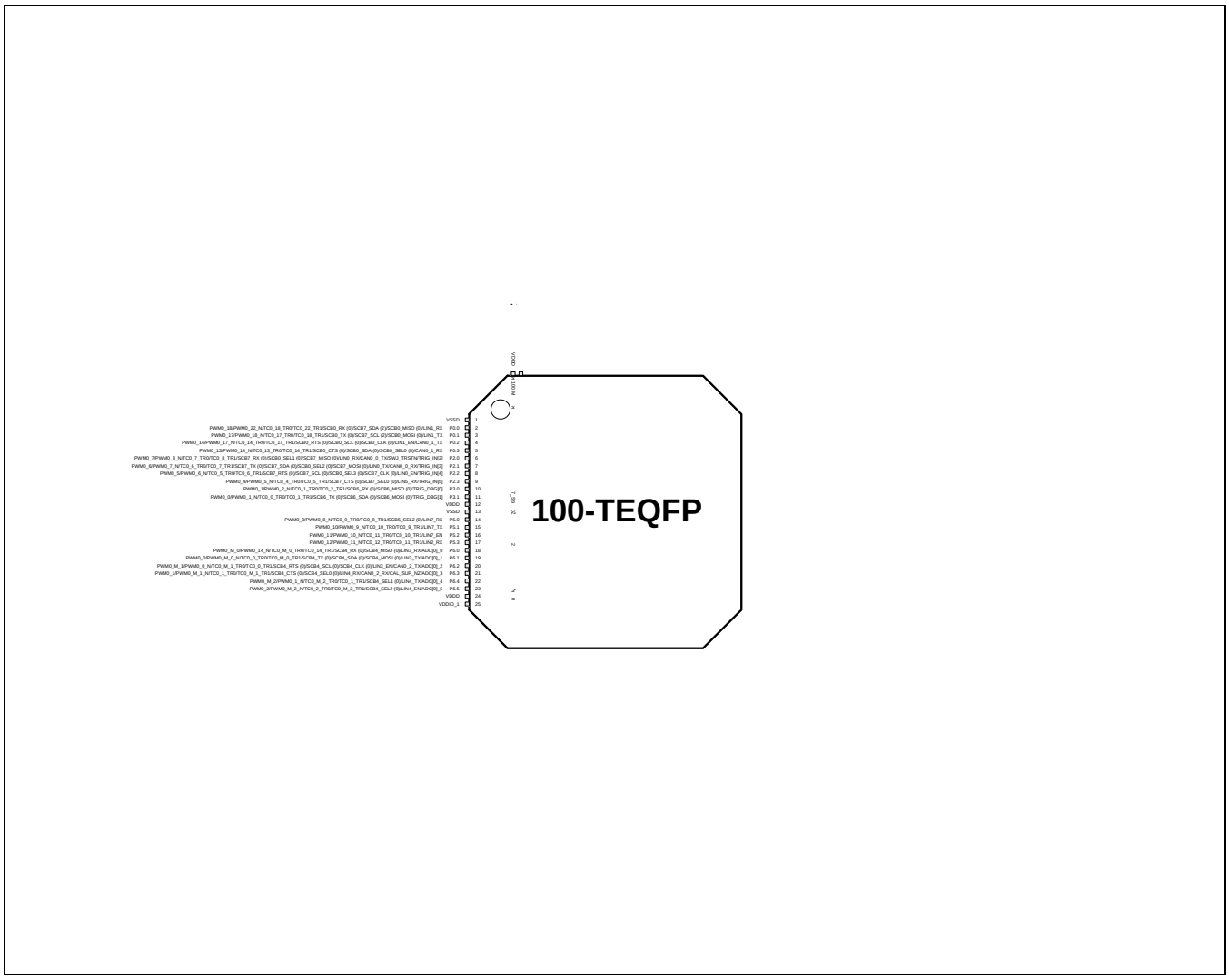


Figure 9-6 100-LQFP pin assignment with alternate functions

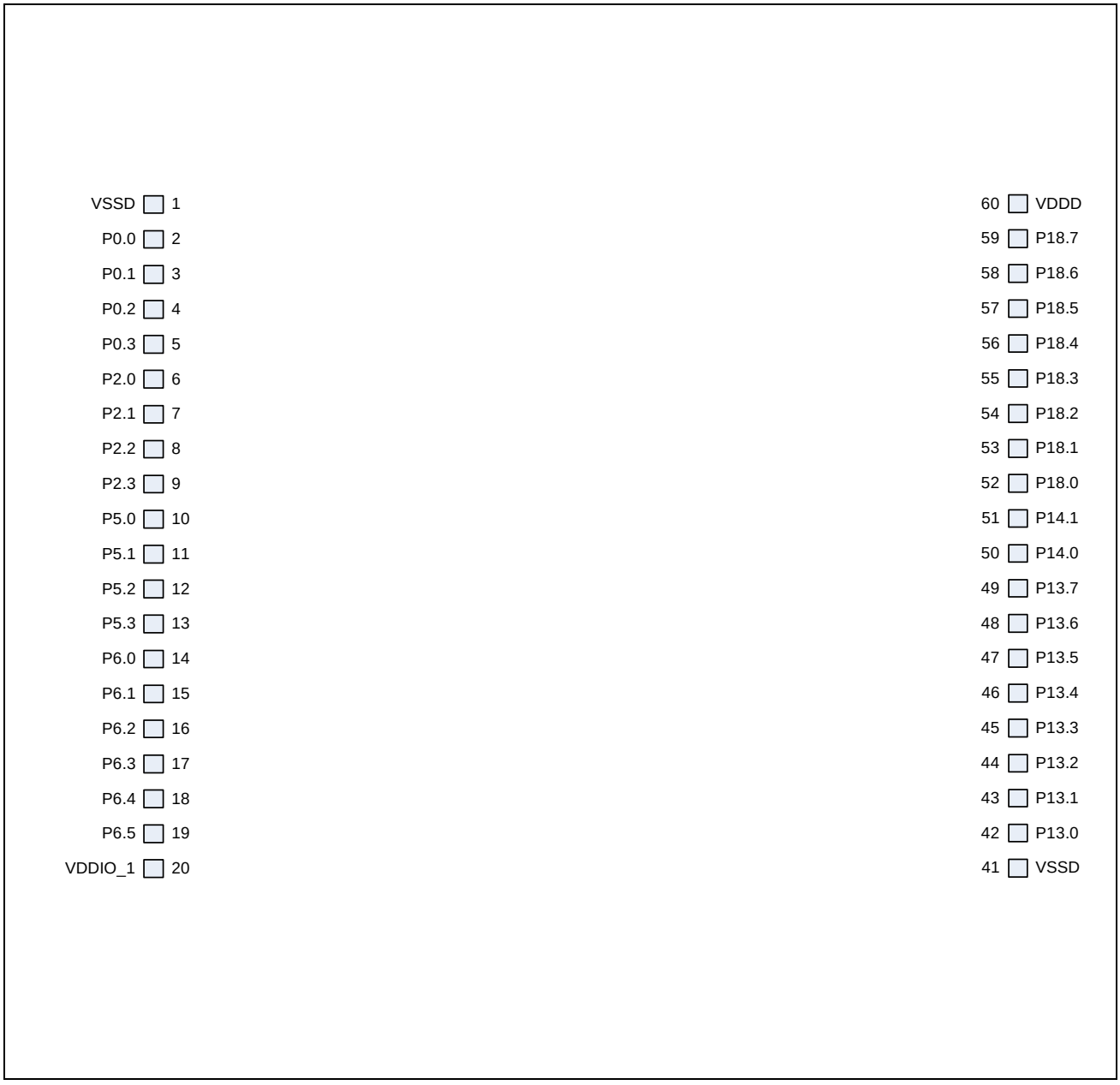


Figure 9-7 80-LQFP pin assignment

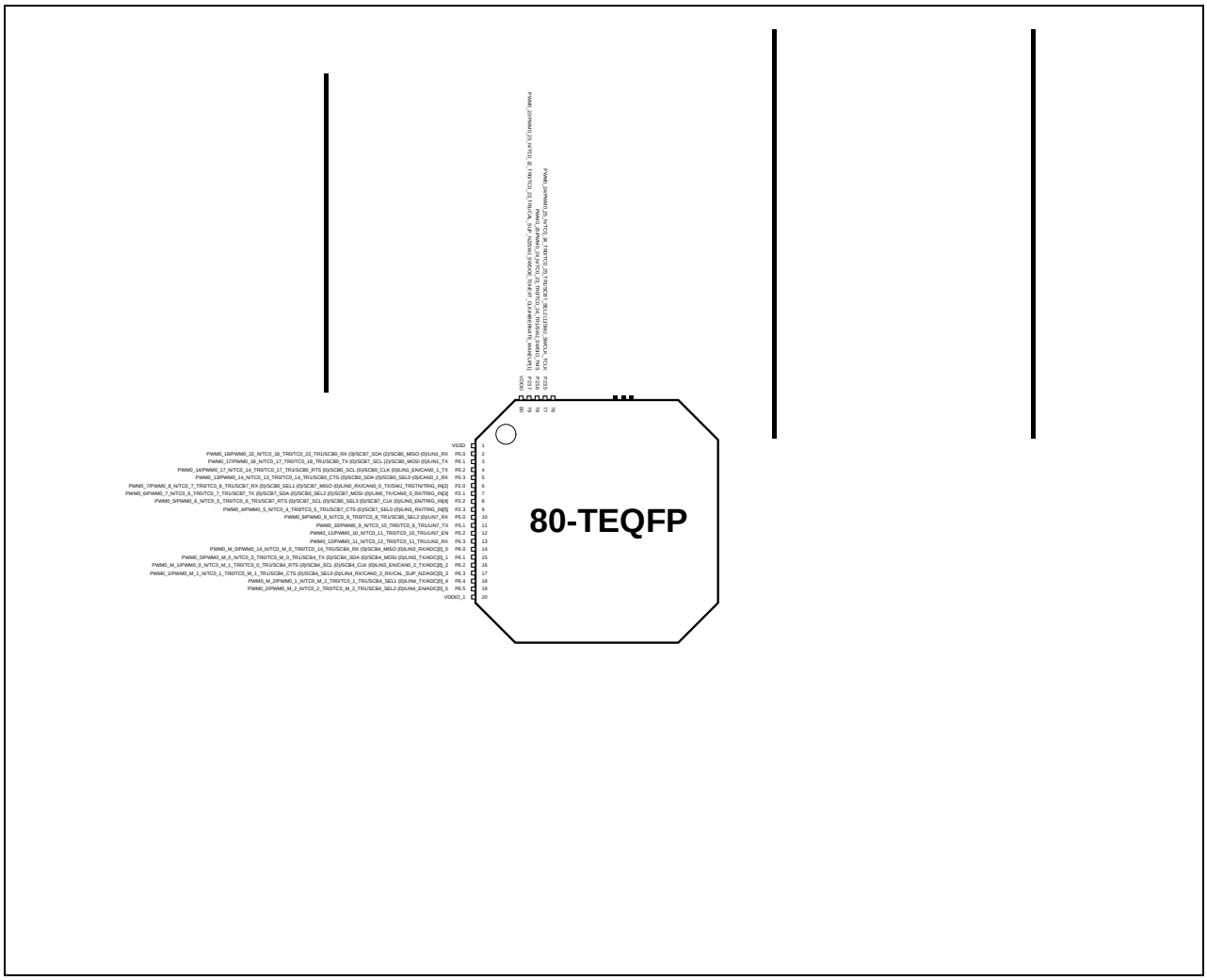


Figure 9-8 80-LQFP pin assignment with alternate functions@À

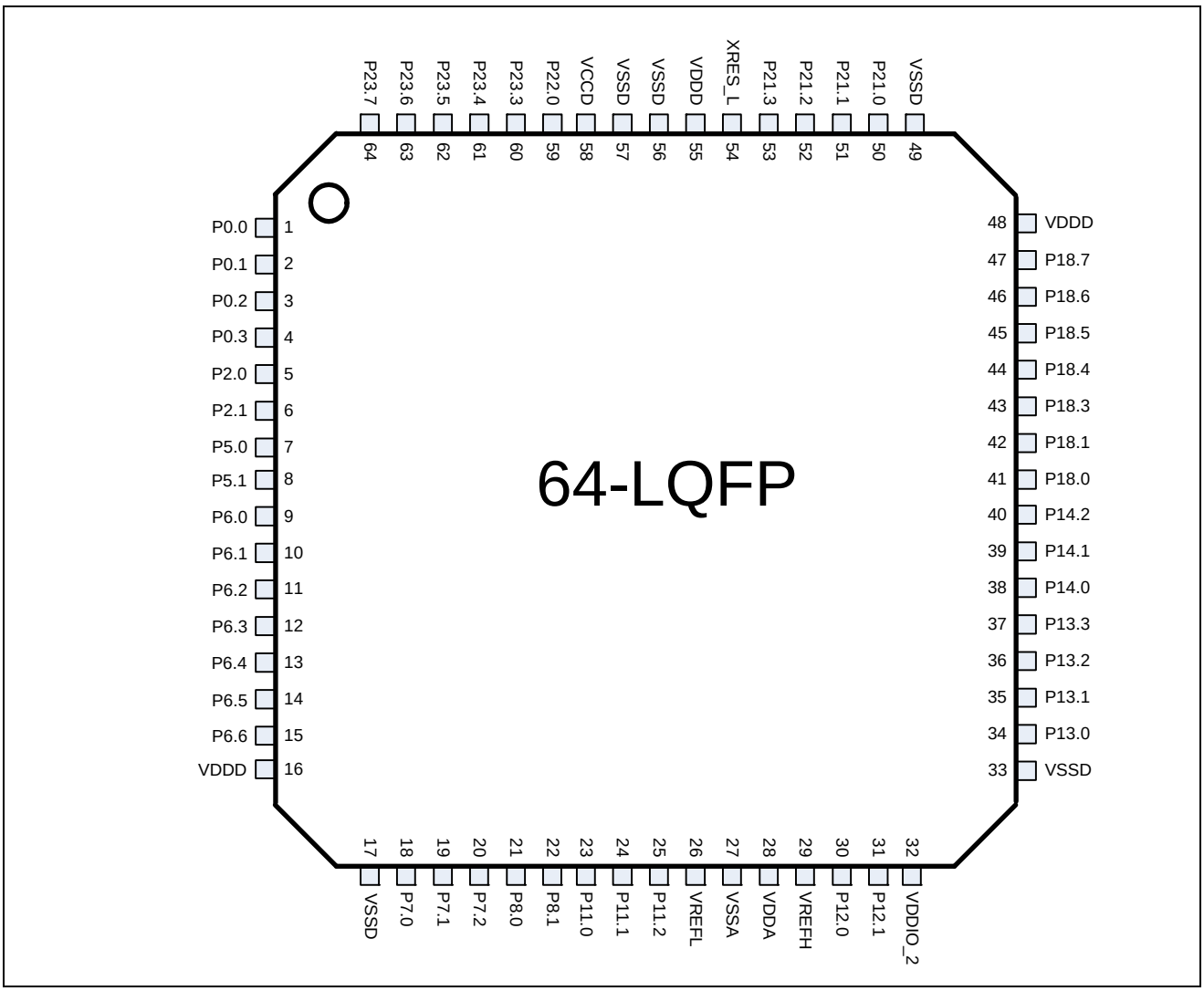


Figure 9-9 64-LQFP pin assignment

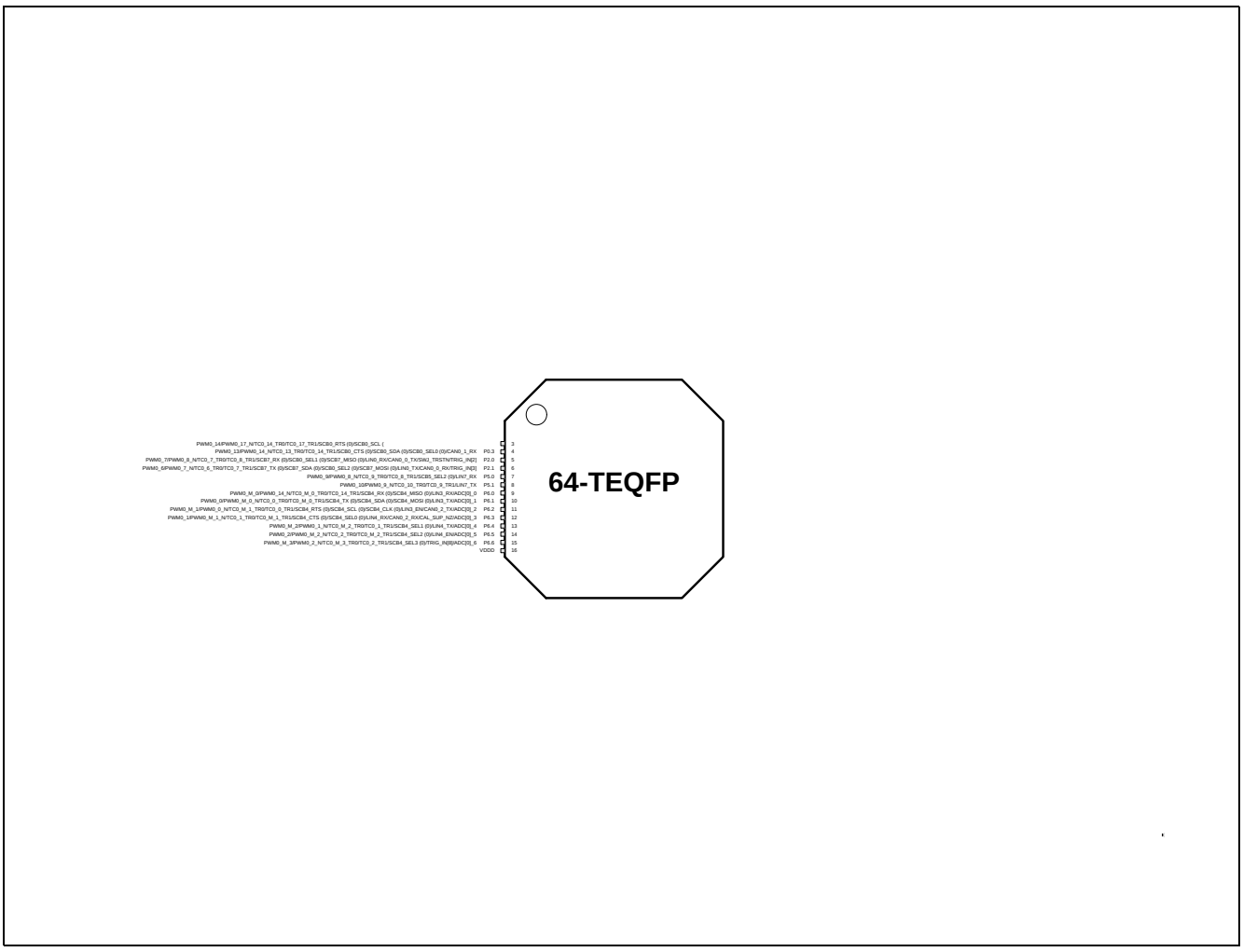


Figure 9-10 64-LQFP pin assignment with alternate functions

10 High-speed I/O matrix connections

Table 10-1 HSIOM connections reference

Name	Number	Description

11 Package pin list and alternate functions

Table 11-1

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[21, 22]

Name		Package					DeepSleep Mapping			Analog	SMARTIO
	HCon#0	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	I/O Type	Pin	Pin	Pin	Pin	Pin	DS #0	DS #1	DS #2		

Notes

Table 10-1

Table 13-2

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[21, 22] *(continued)*

Name		Package					DeepSleep Mapping			Analog	SMARTIO
	HCon#0	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	I/O Type	Pin	Pin	Pin	Pin	Pin	DS #0	DS #1	DS #2		

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[21, 22] *(continued)*

Package				DeepSleep Mapping		
Name	HCon#0	176-LQFP	144-LQFP		Analog	SMARTIO

Table 11-1 Pin selector and alternate pin functions in DeepSleep (DS) Mode, Analog, Smart I/O[21, 22] *(continued)*

Name		Package					DeepSleep Mapping			Analog	SMARTIO
	HCon#0	176-LQFP	144-LQFP	100-LQFP	80-LQFP	64-LQFP	HCon#14	HCon#29	HCon#30		
	I/O Type	Pin	Pin	Pin	Pin	Pin	DS #0	DS #1	DS #2		

12 Power pin assignments

Table 12-1 Power pin assignments

Name	Package					Remarks
	64-LQFP	80-LQFP	100-LQFP	144-LQFP	176-LQFP	

Note

Figure 26-2

13 Alternate function pin assignments

Table 13-1 Alternate pin functions in Active Mode[28, 29]

Name	Active Mapping											
	HCon#8[26]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#26	HCon#27
	ACT#0[27]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7	ACT#8	ACT#9	ACT#14	ACT#15

Notes

Table 10-1

Table 13-2

Table 13-1 Alternate pin functions in Active Mode[28, 29]

Name	Active Mapping



Table 13-1 Alternate pin functions in Active Mode[28, 29]

	Active Mapping											
Name	HCon#8[26]	HCon#9	HCon#10	HCon#11	HCon#16	HCon#17	HCon#18	HCon#19	HCon#20	HCon#21	HCon#26	HCon#27
	ACT#0[27]	ACT#1	ACT#2	ACT#3	ACT#4	ACT#5	ACT#6	ACT#7				

Table 13-2 Pin Mux descriptions

Sl. No.	Pin	Module	Description

14 Interrupts and wake-up assignments

Table 14-1 Peripheral interrupt assignments and wake-up sources

Interrupt	Source	Power Mode	Description

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description

Table 14-1 Peripheral interrupt assignments and wake-up sources *(continued)*

Interrupt	Source	Power Mode	Description

15 Core interrupt types

Table 15-1 Core interrupt types

Interrupt	Source	Power Mode	Description

Note

TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M4F single

17 Triggers group inputs

Table 17-1 Trigger inputs

Input	Trigger Label (TRIG_LABEL)	Description
MUX Group 0		
MUX Group 1		
MUX Group 2		

Table 17-1 Trigger inputs *(continued)*

Input	Trigger Label (TRIG_LABEL)	Description
MUX Group 6		

MUX Group 8

MUX Group 6

MUX Group 7

20 Peripheral clocks

Table 20-1 Peripheral clock assignments

Output	Destination	Description
[redacted]		

Table 20-1 Peripheral clock assignments

21 Faults

Table 21-1 Fault Assignments

Fault	Source	Description

Table 22-1 PPU Fixed Structure Pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description

Table 22-1 PPU Fixed Structure Pairs *(continued)*

Pair No.	PPU Fixed Structure Pair	Address	Size	Description

23 Bus masters

Table 23-1 Bus masters for access and protection control

ID No.	Master ID	Description

24 Miscellaneous configuration

Table 24-1 Miscellaneous configuration for CYT2B7 devices

Sl. No.	Configuration	Number/ Instances	Description
[redacted]			

Table 26-1 Absolute maximum ratings *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
	∑						
							≥
	∑						

Notes

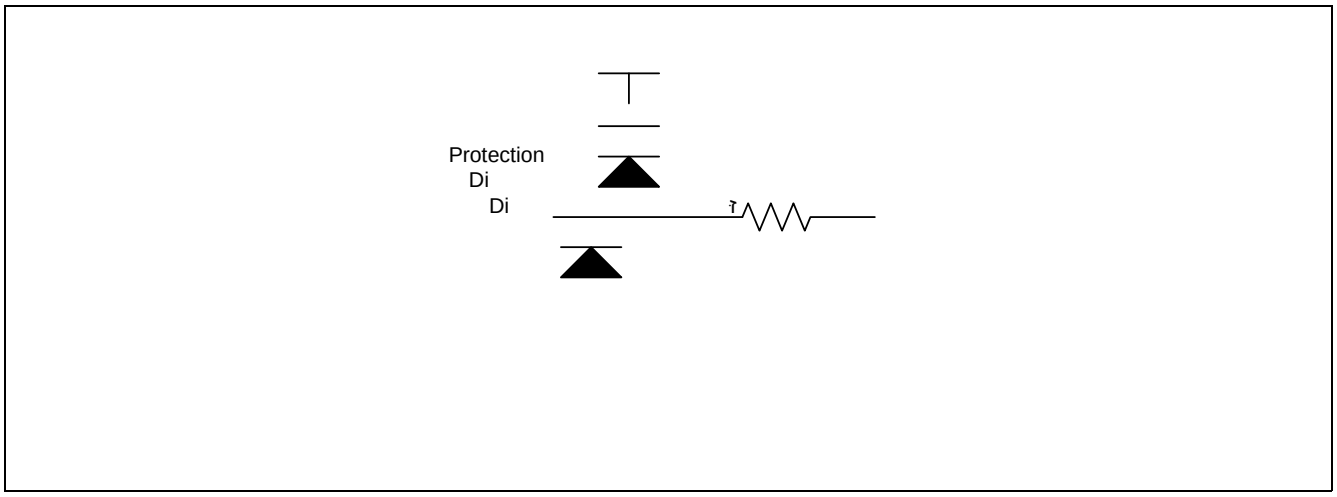


Figure 26-1 Example of a recommended circuit

WARNING:
Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current, or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

TRAVEO™ T2G 32-bit Automotive MCU

Based on Arm® Cortex®-M4F single

26.3 DC specifications

Table 26-3 DC specifications, CPU current and transition time specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Note

Table 26-3 DC specifications, CPU current and transition time specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Regulator specifications							

26.4 Reset specifications

Table 26-4 XRES_L reset

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
XRES_L DC specifications							
						Ω	
XRES_L AC specifications							

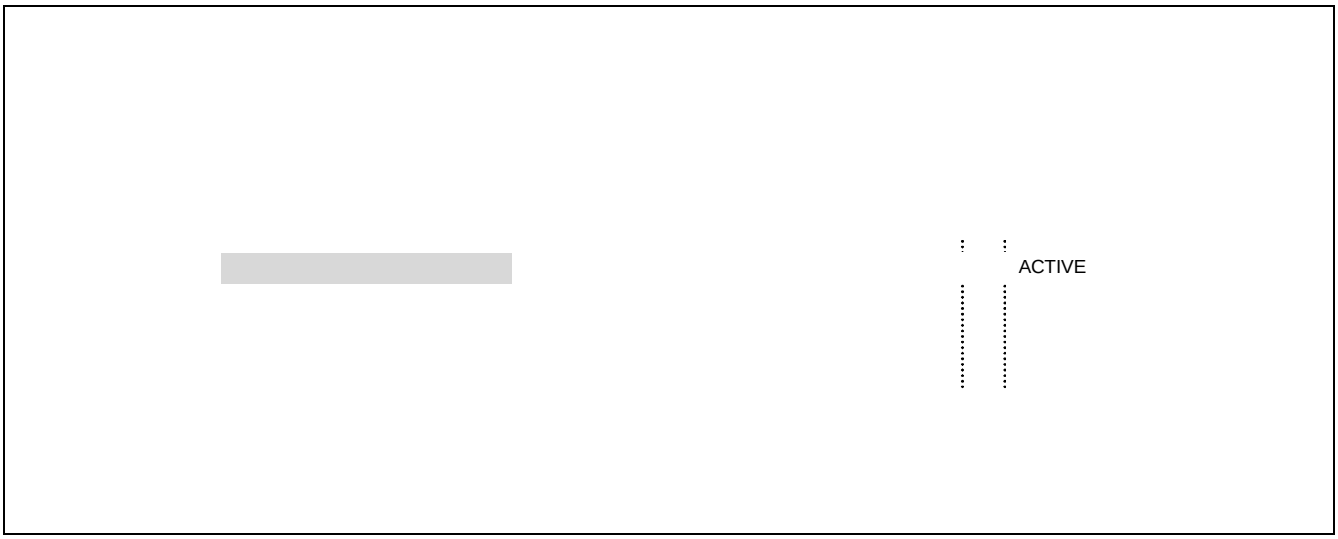


Figure 26-3 Reset sequence

26.5 I/O

All specifications are valid for –40 °C T_A 125 °C and for 2.7 V to 5.5 V except where noted.

Table 26-5 I/O specifications

Spec ID	Parameter	Min	Typ	Max	Units	Details/Conditions
GPIO_STD	**Specifications for ports P1 through P.5(5Pa)44.e61TD SpUnionrG1.5GPIO_Smeter**					

≤

≤

Ω

Ω

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤
							≤ ≤
							≤
							≤ ≤
							≤
GPIO_ENH specifications only for P0							
							≤ ≤
							≤ ≤
							≤
							≤
							≤ ≤
							≤
							≤ ≤
							≤
							≤ ≤

Table 26-5 I/O specifications

≤

≤ ≤

≤

≤ ≤

Ω

Ω

≤ ≤

Ω

Table 26-5 I/O specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤ ≤
							≤
GPIO input specifications							

Note

26.6 Analog peripherals

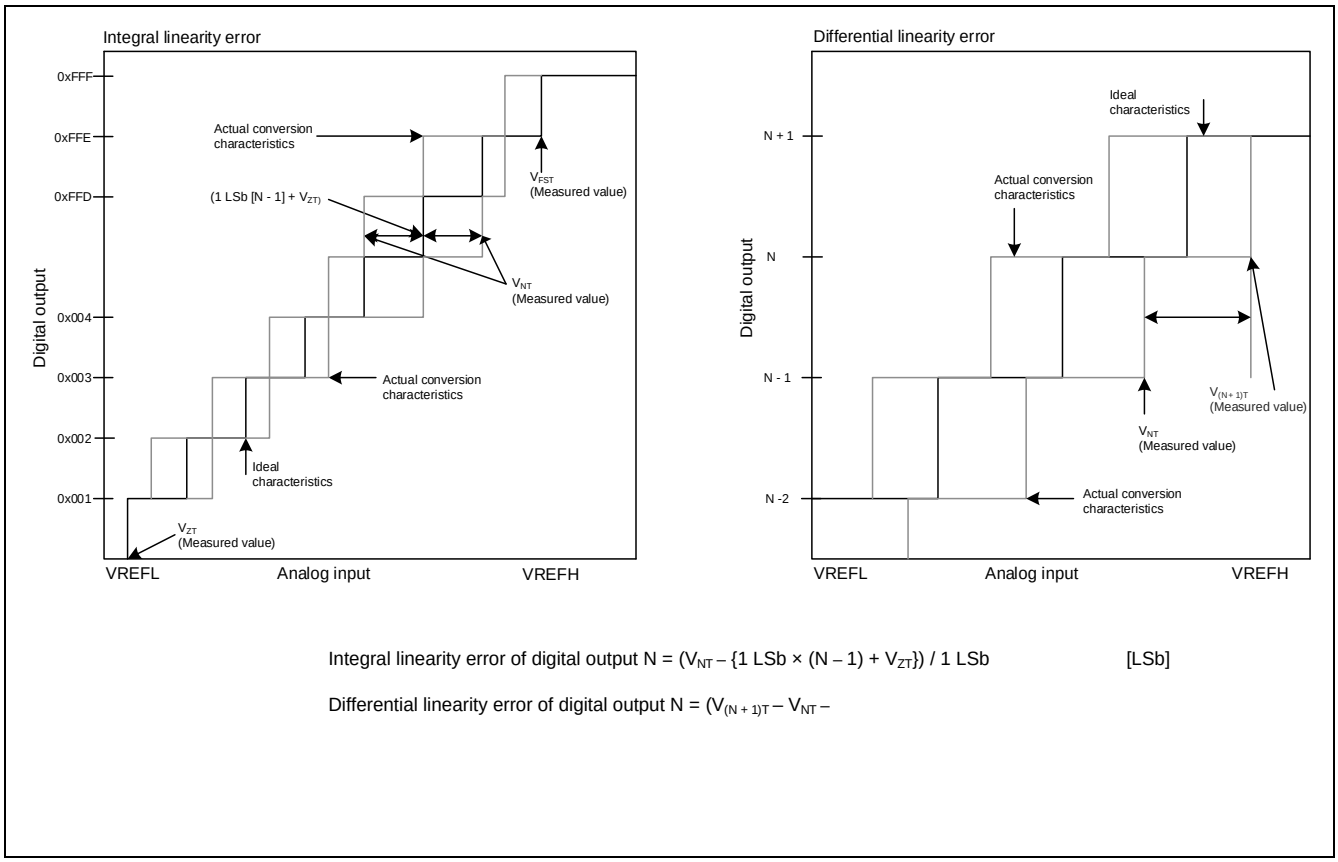
26.6.1 SAR ADC

Figure 26-4 ADC characteristics and error definitions

Table 26-6 12-Bit SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
						Ω	

26.6.2 Calculating the impact of neighboring pins



Integral linearity error of digital output N = (V_{NT} – {1 LSb × (N – 1) + V_{ZT}}) / 1 LSb [LSb]

Differential linearity error of digital output N = ($V_{(N+1)T}$ – V_{NT} –

Figure 26-5 Integral and differential linearity errors

Table 26-7 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤ ≤
							≤ ≤
							≤ ≤
							≤
							≤ ≤
							≤
						Ω	
						Ω	
						Ω	
						Ω	
							≤ ≤
							≤ ≤
							≤ ≤

Table 26-7 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤ ≤
							≤ ≤

26.6.3 Temperature sensor

Table 26-8 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤ ≤ ≤ ≤ ≤ ≤
							≤ ≤ ≤ ≤ ≤ ≤

26.6.4 Voltage divider accuracy

Table 26-9 Voltage divider accuracy

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

26.7 AC specifications

Figure 26-7

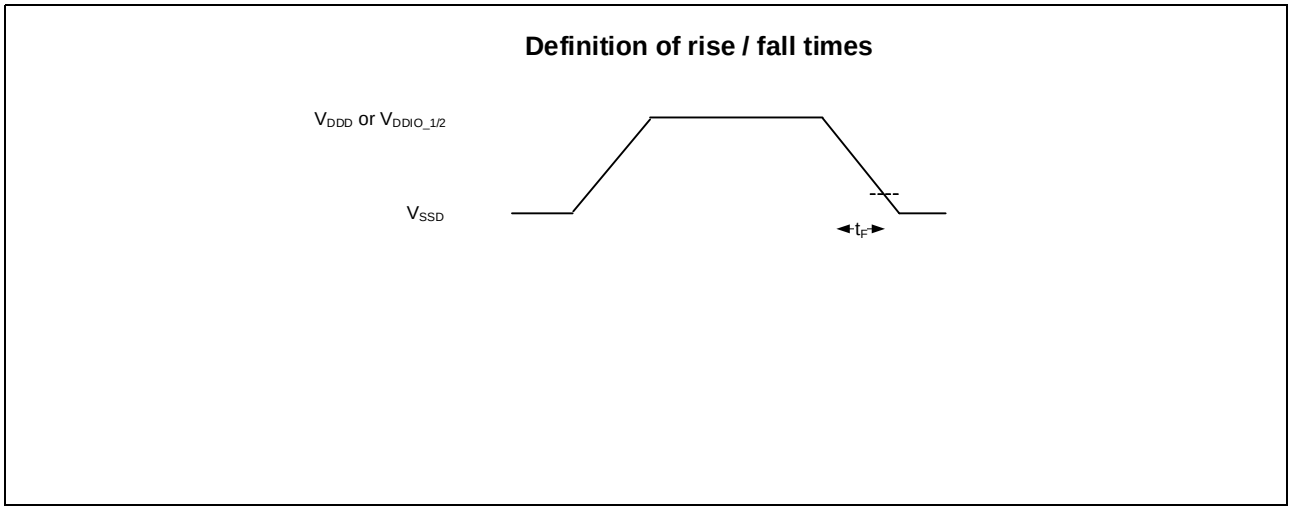


Figure 26-7 AC timings specifications

Table 26-11 Serial communication block (SCB) specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
					100	MHz	
I^2C Interface-Standard-mode							
I^2C Interface-Fast-mode							

Table 26-11 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							Ω
							Ω

I^2C Interface-Fast-Plus mode



>= 0x]

Table 26-11 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SPI Interface Slave (externally clocked) [Conditions: drive_sel<1:0>= 0x]							

Table 26-11 Serial communication block (SCB) specifications *(continued)*

Spec ID	Parameter	Description	Min
UART Interface			

Figure 26-9 I^2C timing diagrams

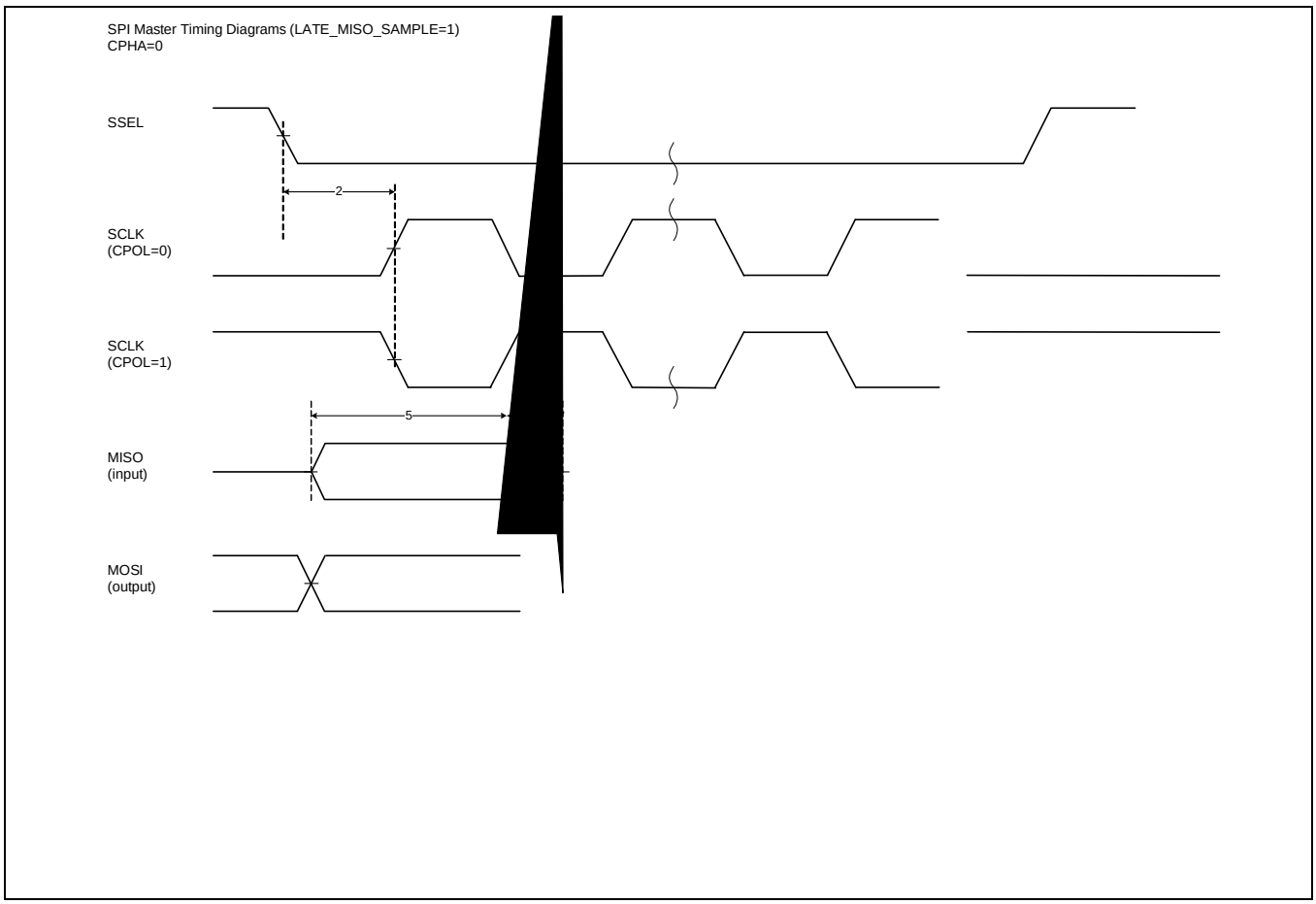
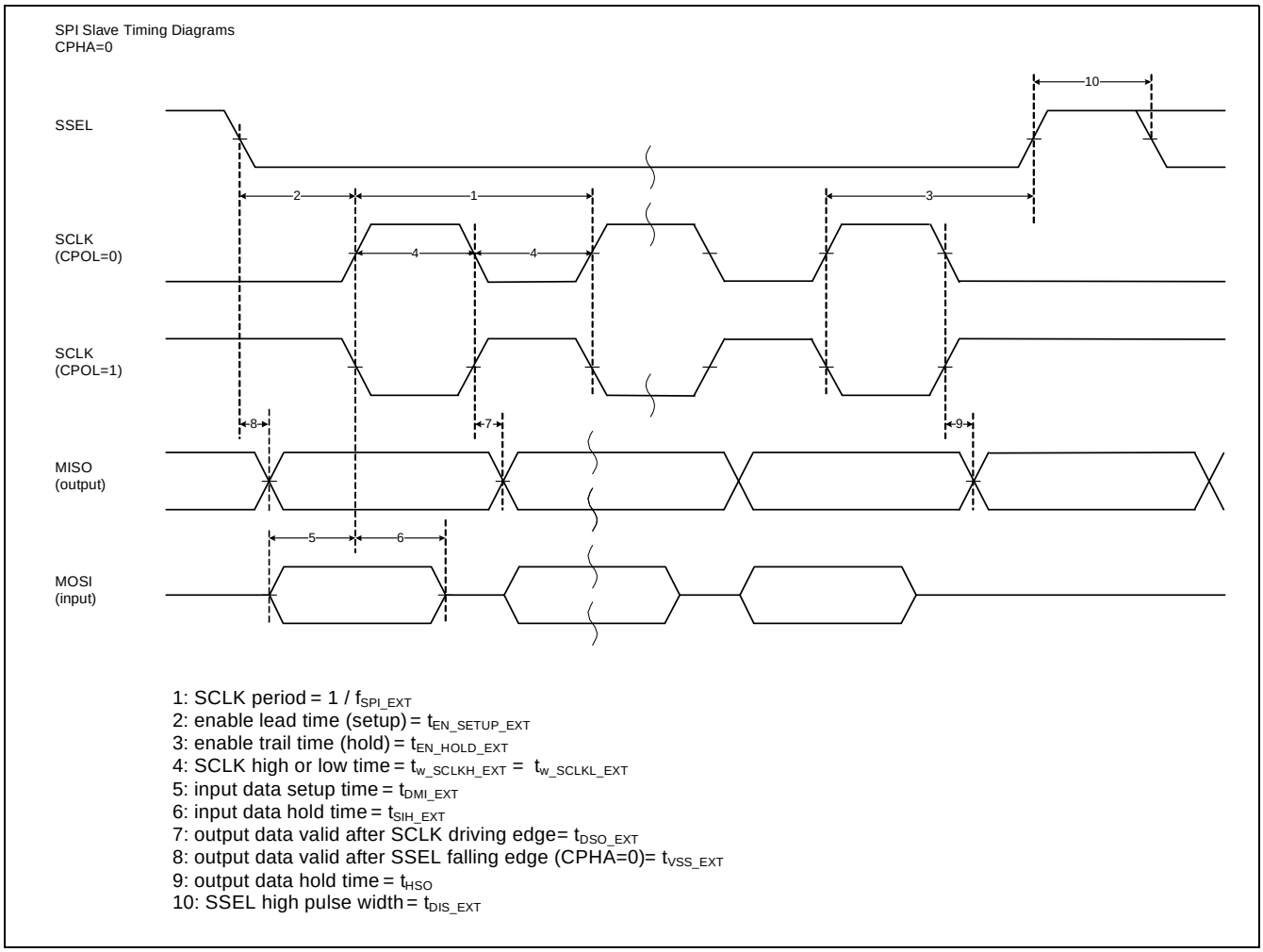


Figure 26-10 SPI master timing diagrams with LOW clock phase

Figure 26-11 SPI master timing diagrams with HIGH clock phase



1: SCLK period = 1 / f_{SPI_EXT}
2: enable lead time (setup) = $t_{EN_SETUP_EXT}$
3: enable trail time (hold) = $t_{EN_HOLD_EXT}$
4: SCLK high or low time = $t_{w_SCLKH_EXT}$ = $t_{w_SCLKL_EXT}$
5: input data setup time = t_{DMI_EXT}
6: input data hold time = t_{SIH_EXT}
7: output data valid after SCLK driving edge= t_{DSO_EXT}
8: output data valid after SSEL falling edge (CPHA=0)= t_{VSS_EXT}
9: output data hold time = t_{HSO}
10: SSEL high pulse width = t_{DIS_EXT}

Figure 26-12 SPI slave timing diagrams with LOW clock phase

Figure 26-13 SPI slave timing diagrams with HIGH clock phase

26.8.1 LIN specifications

Table 26-12 LIN specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

26.8.2 CAN FD specifications

Table 26-13 CAN FD specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
							≤
							≤

26.9 Memory

Table 26-14 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Table 26-15 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

≥

26.10 System resources

Table 26-16 System resources

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
Power-on-reset specifications							
High-voltage BOD (HV BOD) specifications							

Low-voltage BOD (LV BOD) specifications

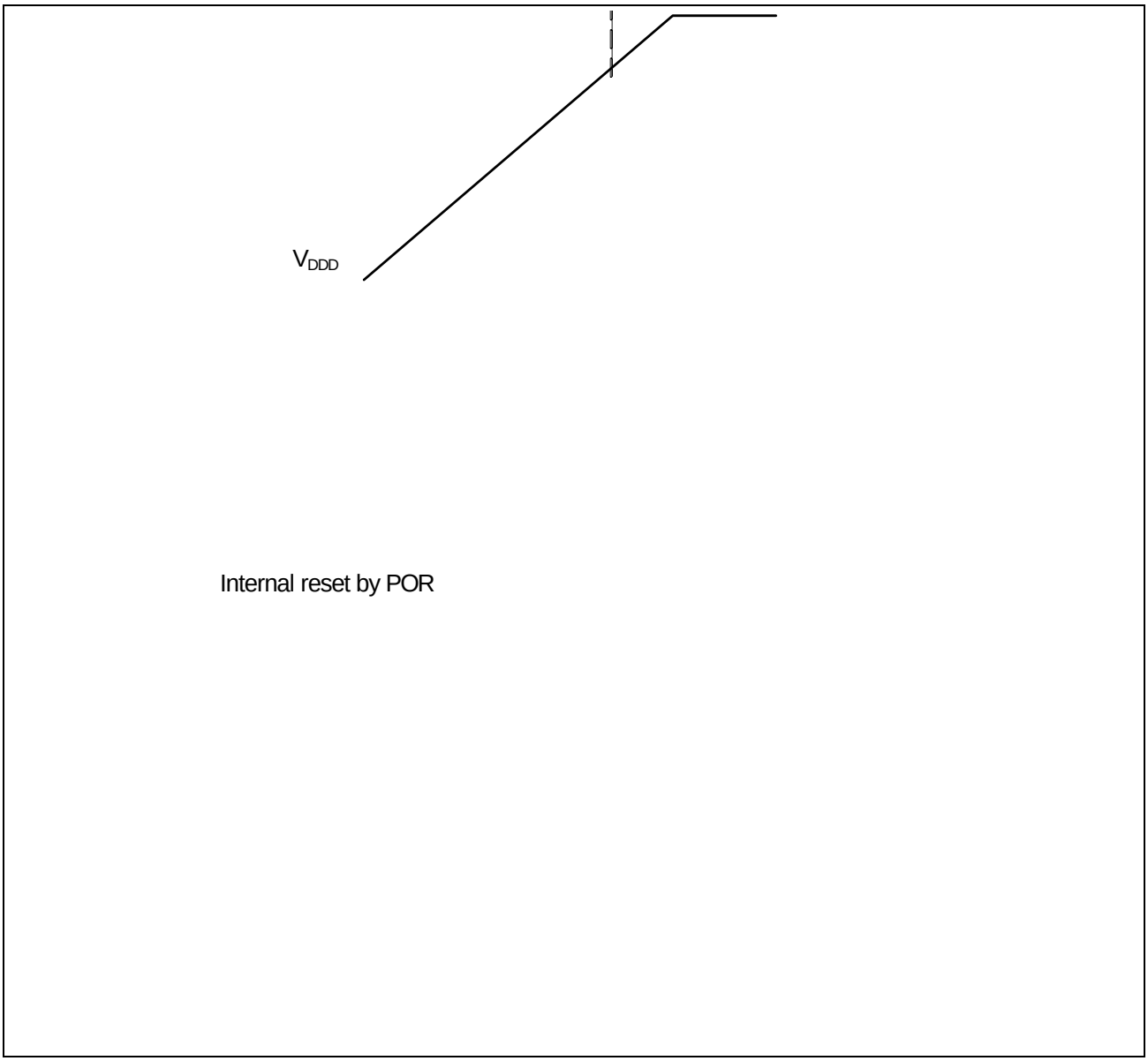


Figure 26-15 POR specifications

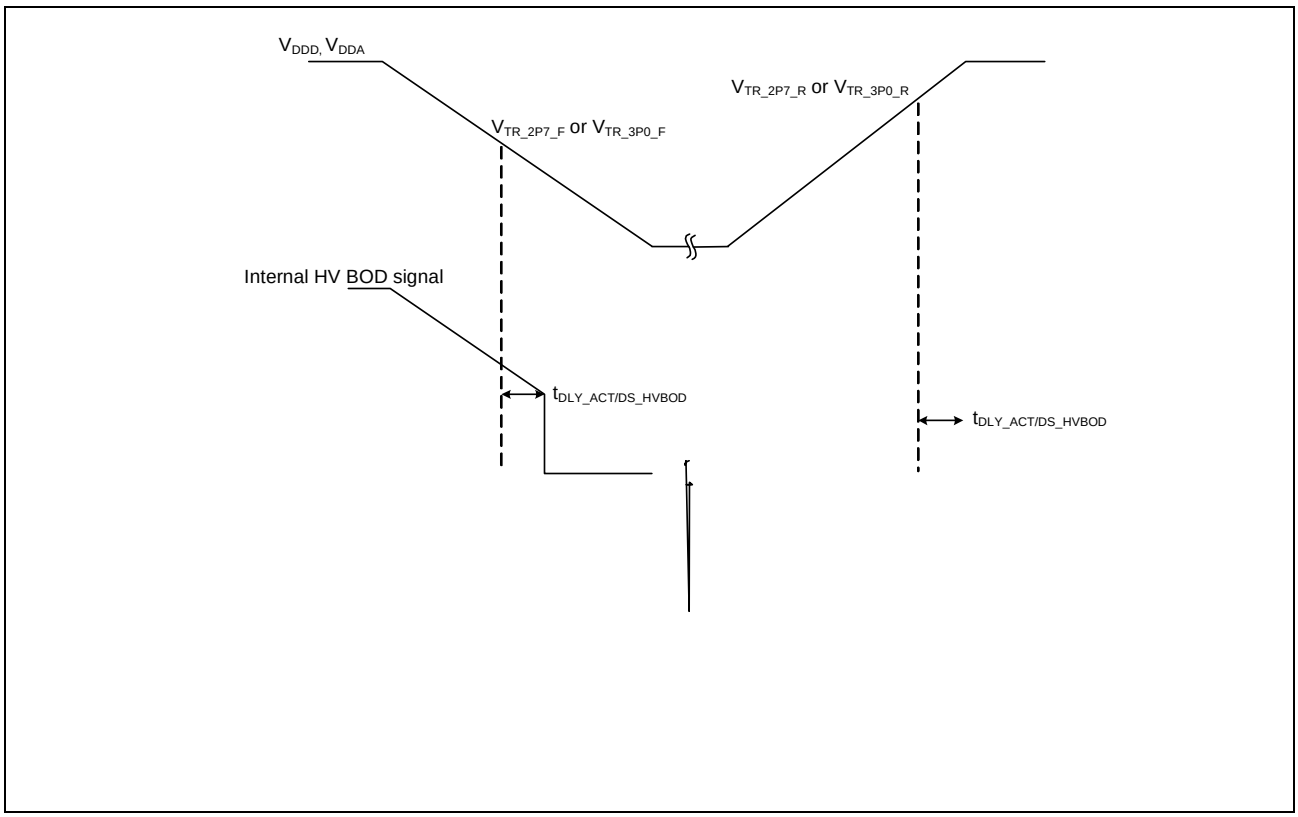


Figure 26-16 High-voltage BOD specifications

Figure 26-17 Low-voltage BOD specifications

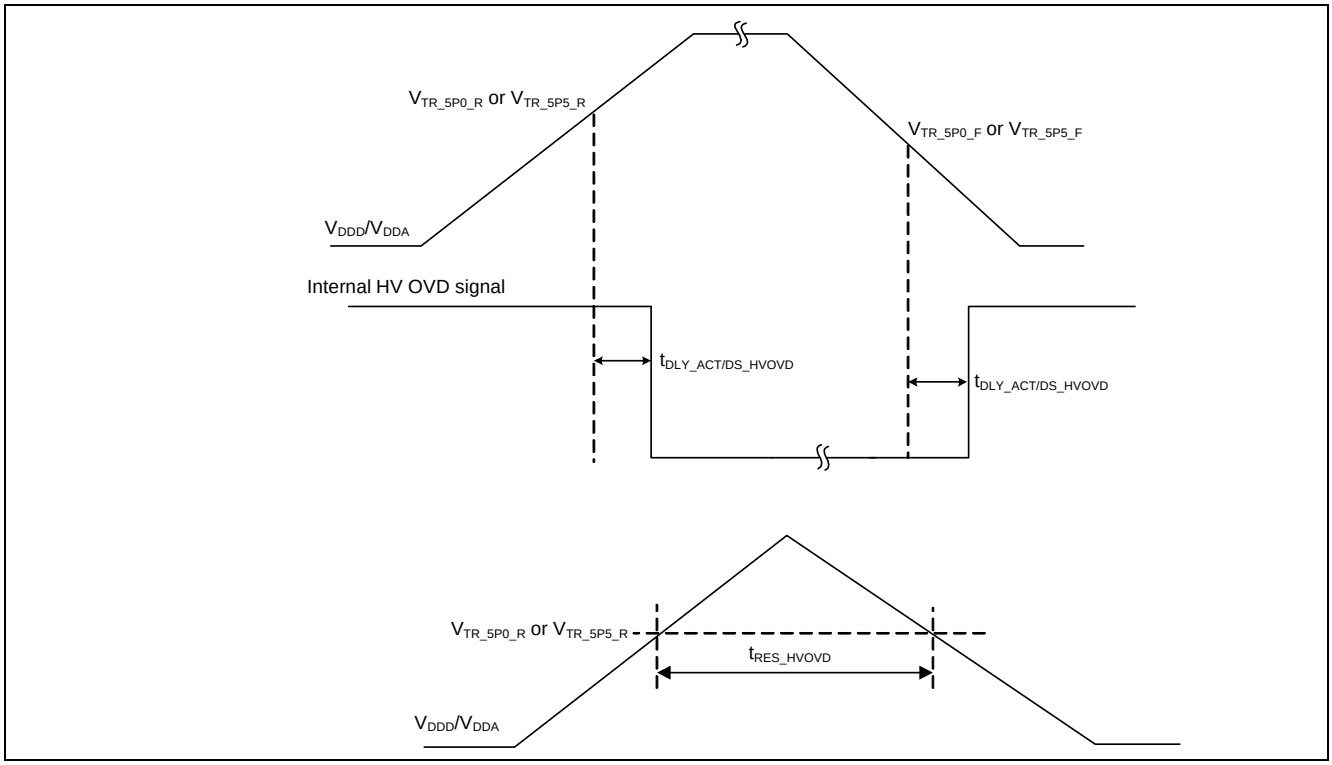


Figure 26-18 High-voltage OVD specifications

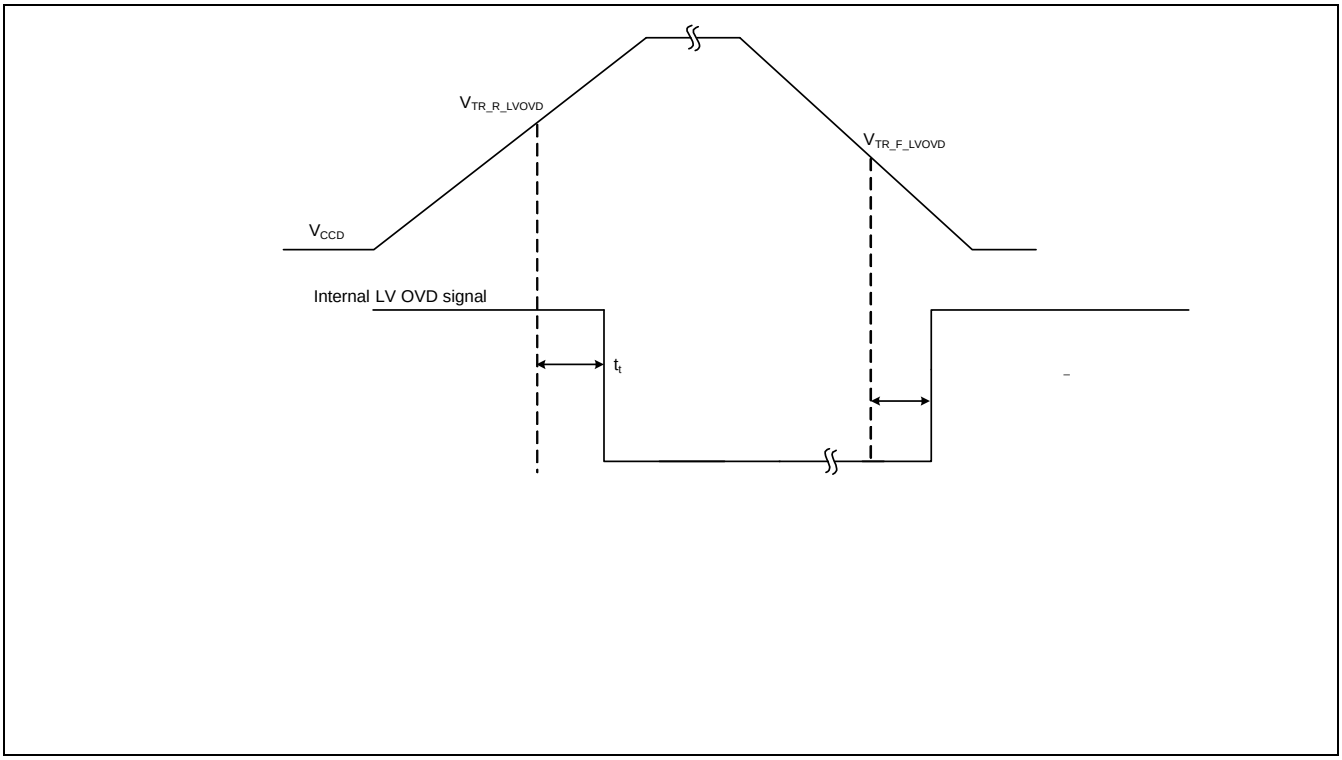


Figure 26-19 Low-voltage OVD specifications

Figure 26-20 LVD specifications

26.11 Debug

26.11.2 JTAG

Table 26-18 JTAG AC specifications [Conditions: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

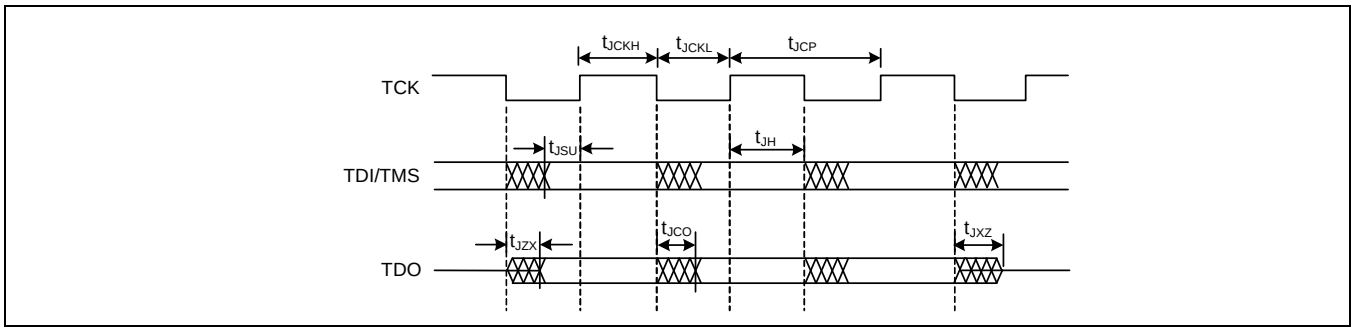


Figure 26-21 JTAG timing diagram

26.11.3 Trace

Table 26-19 Trace specifications [Conditions: drive_sel<1:0>= 00]

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

26.12 Clock specifications

Table 26-24 ECO specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
		Ω				Ω	

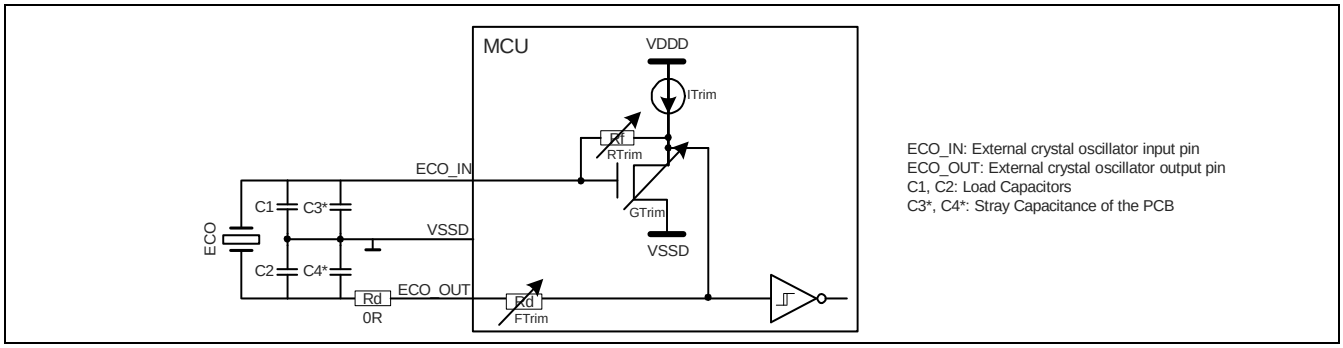


Figure 26-22 ECO connection scheme

Table 26-25 PLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Notes

Table 26-25 PLL specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Table 26-26 FLL specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

Figure 26-23 WCO connection scheme

Table 26-28 External clock input specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions

26.12.1 Clock timing diagrams

Figure 26-24 ECO to PLL or FLL diagram

Figure 26-25 WCO to FLL Diagram

Table 26-29 MCWDT timeout specifications

27 Ordering information

Table 27-1

Table 27-1 CYT2B7 ordering information

Device Code	Ordering Code[61]	Package	Code-flash (KB)	Work-flash (KB)	RAM (KB)	ADC Channels	SCB Channels	LIN Channels	CANFD Channels	eSHE/HSM	Temperature Grade	JTAG ID CODE

Notes

27.1 Part number nomenclature

Table 27-2 Device code nomenclature

Field	Description	Value	Meaning

Table 27-3 Ordering code nomenclature

Field	Description	Value	Meaning

28 Packaging

Table 28-1

Table 28-1 Package Information

Package	Dimensions	Contact/Lead pitch

Table 28-3 Solder Reflow Peak Temperature, Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	Maximum Peak Temperature (°C)	Maximum Time at Peak Temperature (seconds)	MSL

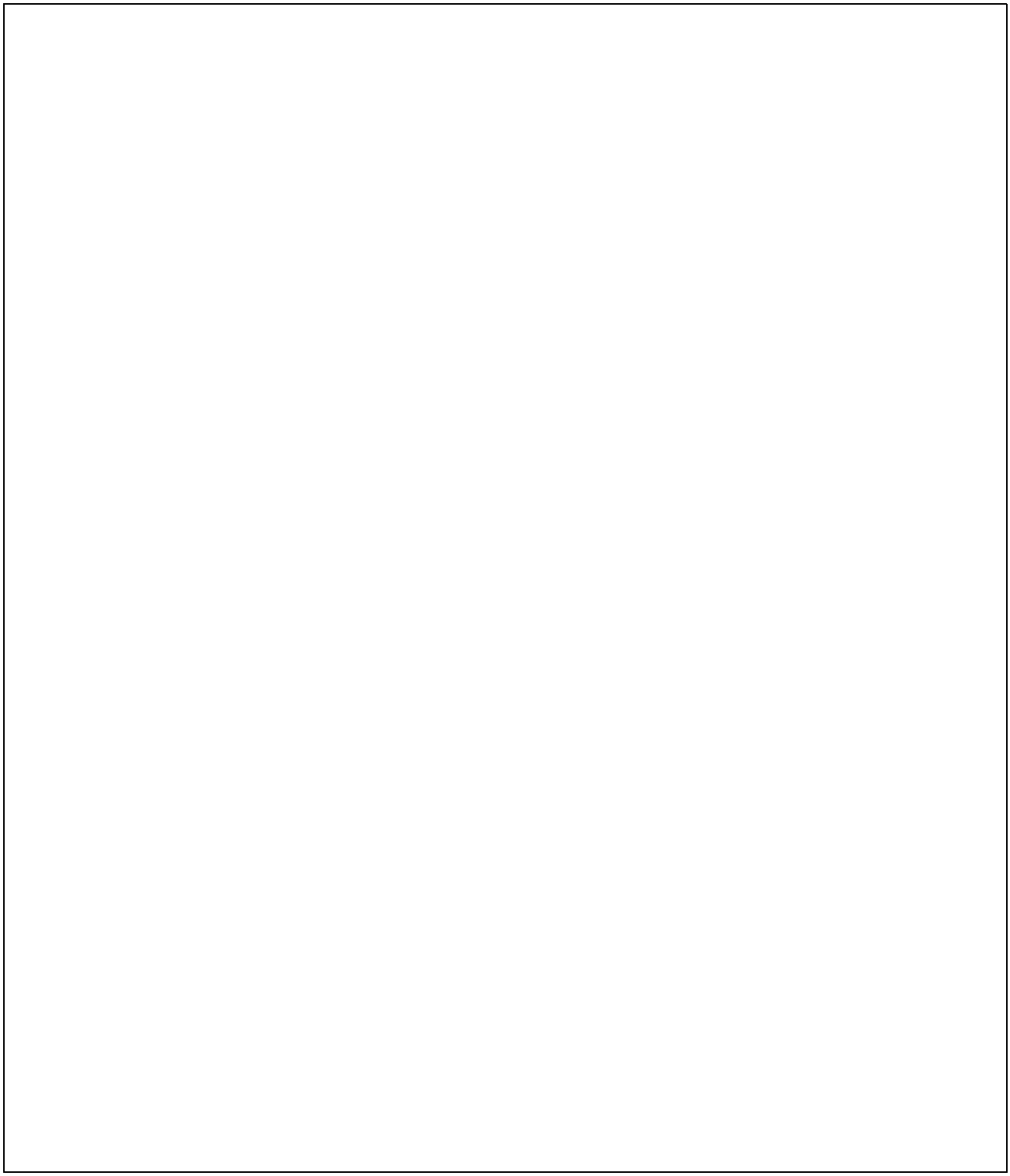


Figure 28-1 176-LQFP package outline

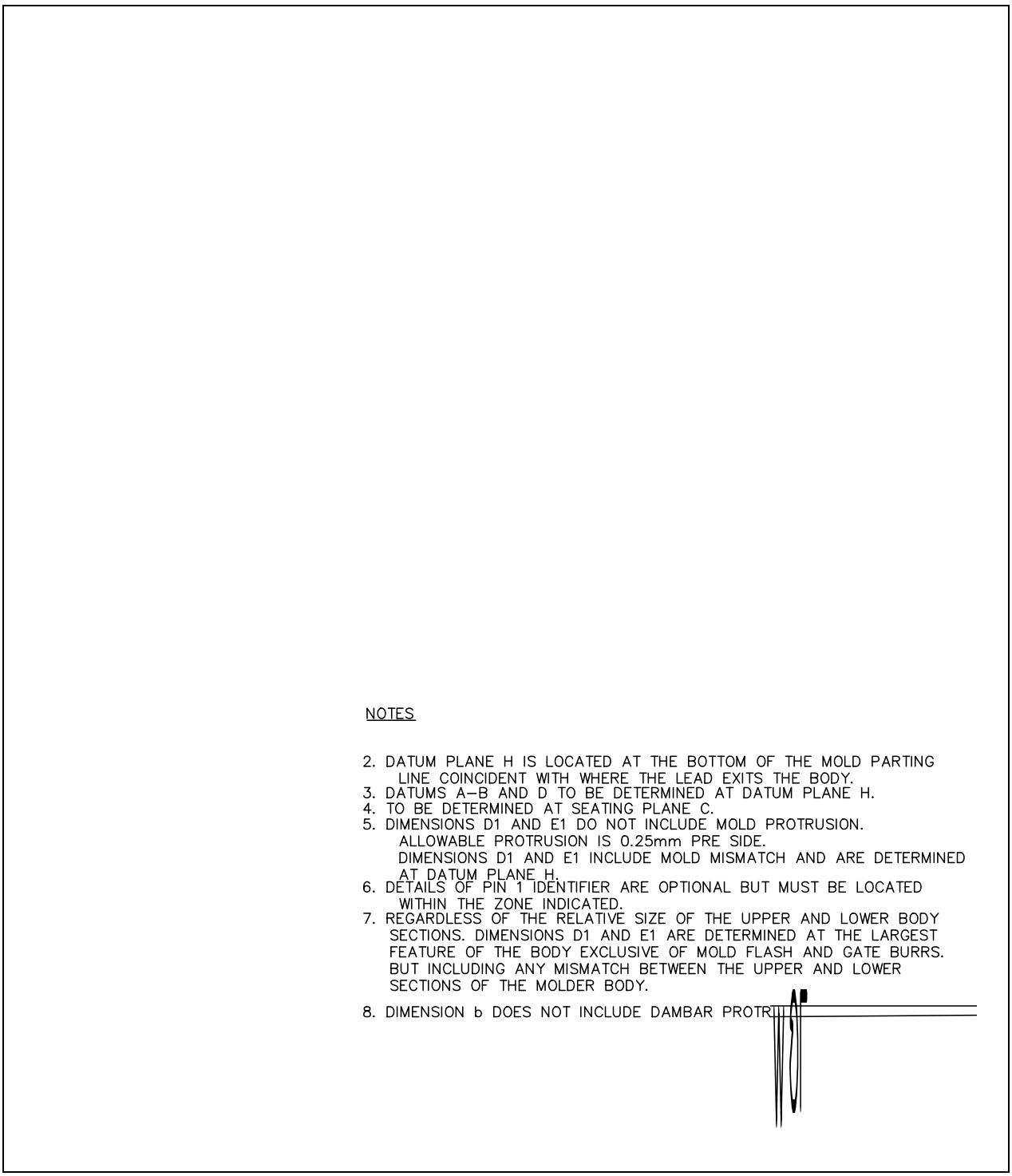
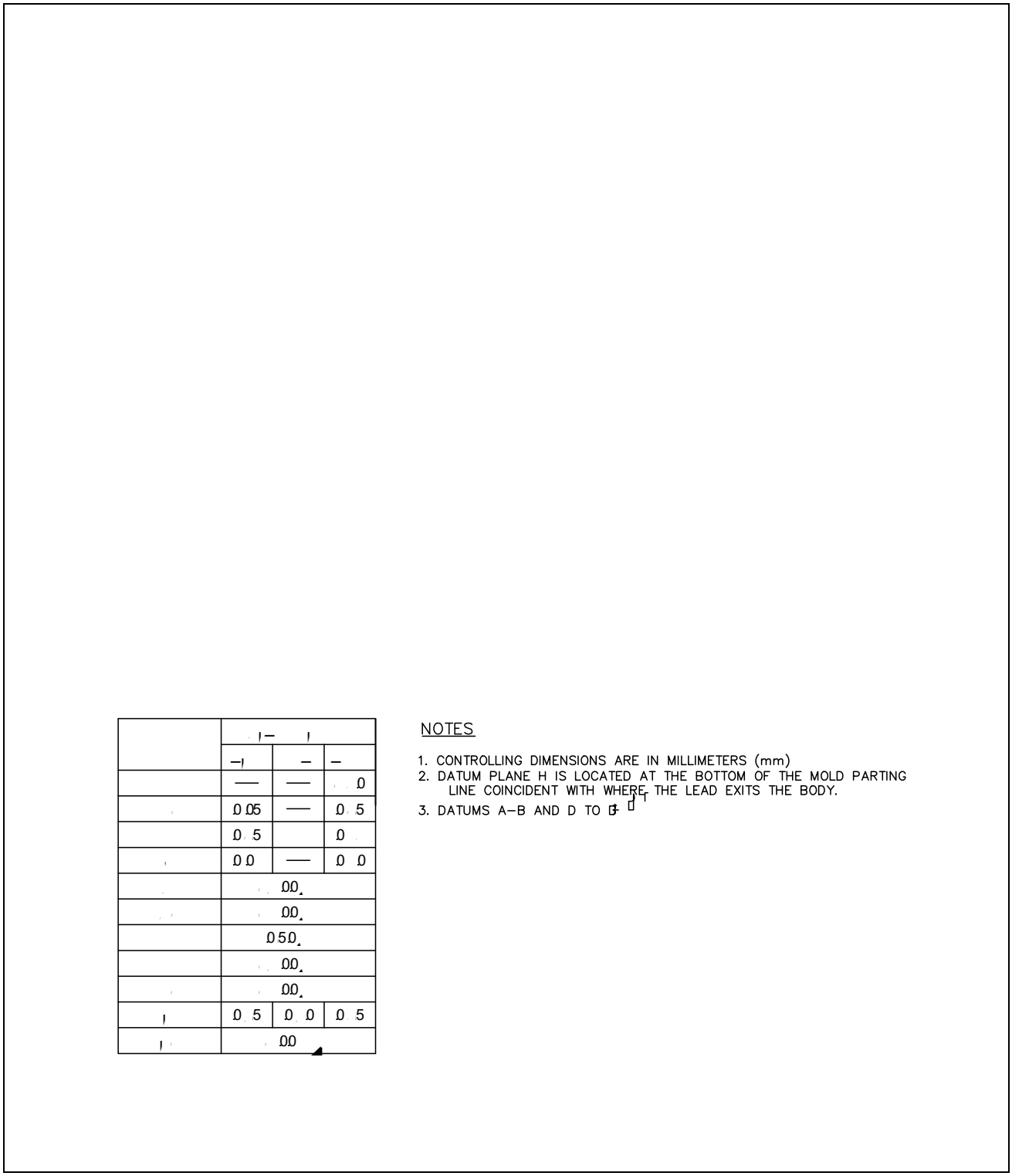


Figure 28-2 144-LQFP package outline



Figure 28-3 100-LQFP package outline

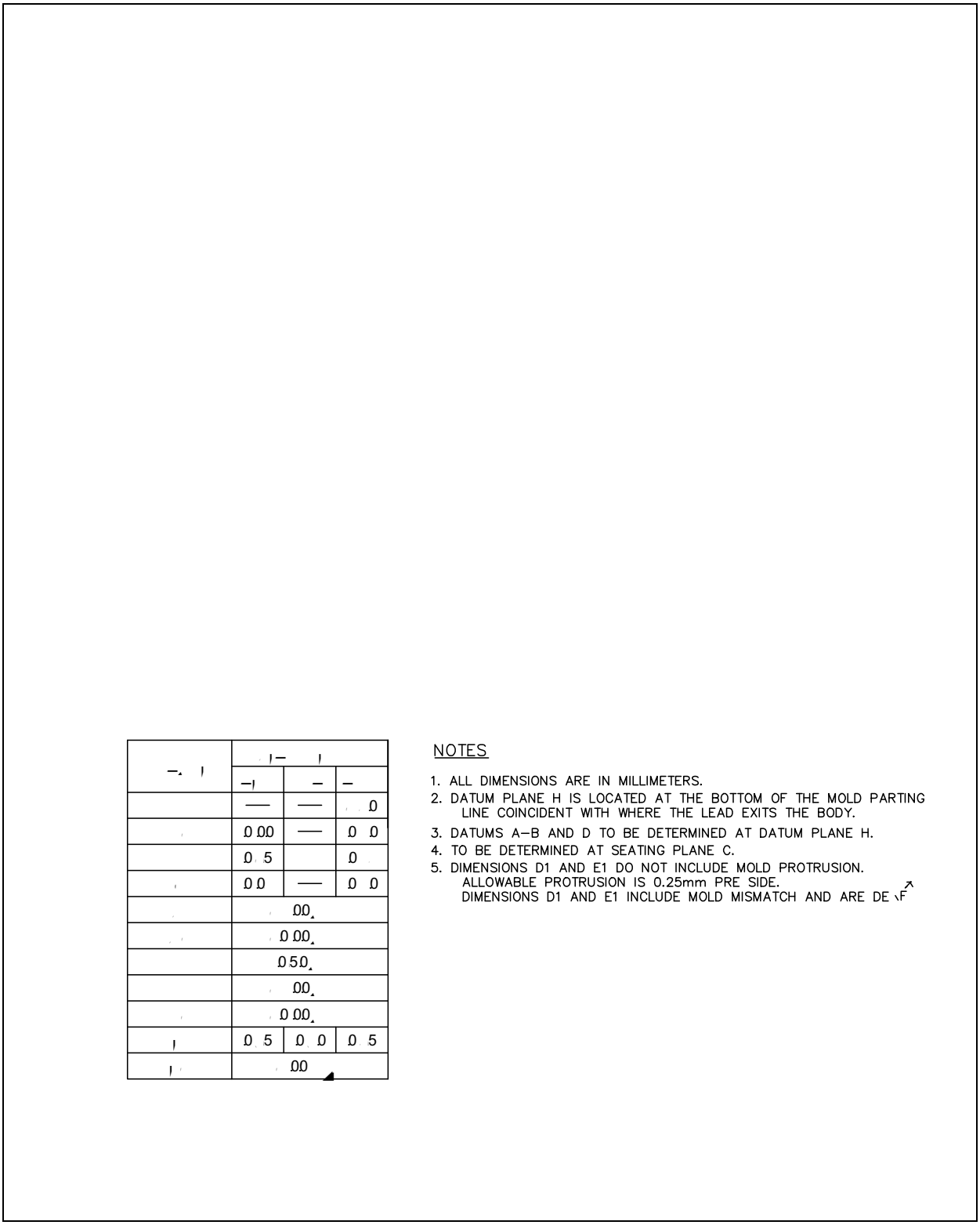


	—	—	0
	0.05	—	0.5
	0.5		0
	0.0	—	0.0
	0.0		
	0.0		
	0.50		
	0.0		
	0.0		
	0.5	0.0	0.5
	0.0		

NOTES

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm)
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A–B AND D TO

Figure 28-4 80-LQFP package outline



	—	—	0
	0.00	—	0.20
	0.15		0
	0.20	—	0.20
	0.00		
	0.00		
	0.50		
	0.00		
	0.00		
	0.15	0.20	0.15
	0.00		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A–B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DE F

Figure 28-5 64-LQFP package outline

29 Appendix

29.1 Bootloading or end-of-line programming

Figure 29-1 Bootloading sequence

Table 29-1 CAN interface details

Sl. No.	CAN interface	Configuration

Figure 29-2 MCU to CAN transceiver connections

Table 29-2 LIN interface details

Sl. No.	LIN interface	Configuration

Figure 29-3 MCU to LIN transceiver connections

29.2 External IP revisions

Table 29-3 IP revisions

Module	IP	Revision	Vendor

30 Acronyms

Table 30-1 Acronyms used in the Document

Acronym	Description	Acronym	Description

31 Errata

Part Numbers Affected

Part Number

CYT2B7 Qualification Status

CYT2B7 Errata Summary

1. Crypto LSL1, LSR1, LSL1_WITH_CARRY, & LSR1_WITH_CARRY instructions may work incorrectly in certain scenarios

Problem Definition

Parameters Affected

Trigger Condition(s)

Scope of Impact

Workaround

Fix Status

2. Crypto MEM_BUF may be corrupted

Problem Definition

Parameters Affected

Trigger Condition(s)

Scope of Impact

Workaround

Fix Status

3. ConfigureFmInterrupt API assumes a parameter with 8 bytes boundary, but actual boundary is 4 bytes

Problem Definition

Parameters Affected

Trigger Condition(s)

10. WDT service can be missed

Problem Definition

Parameters Affected

Trigger Condition(s)

Scope of Impact

Workaround

14.WDT reset causes loss of SRAM retention	
Problem Definition	
Parameters Affected	
Trigger Condition(s)	
Scope of Impact	
Workaround	
Fix Status	

15.Crypto ECC errors may be set after boot with application authentication	
Problem Definition	
Parameters Affected	
Trigger Condition(s)	
Scope of Impact	
Workaround	
Fix Status	

16.Incomplete erase of Code Flash cells could happen Erase Suspend / Erase Resume is used along with Erase Sector operation in Non-Blocking mode	
Problem Definition	
Parameters Affected	
Trigger Condition(s)	
Scope of Impact	
Workaround	
Fix Status	

17.Limitation for keeping the port state from peripheral IP after wakeup from DeepSleep	
Problem Definition	
Parameters Affected Trigger Condition(s) Scope of Impact Workaround Fix Status	

18.Limitation of clock configuration before entering DeepSleep mode.

Problem Definition

Parameters Affected

Trigger Condition(s)

Scope of Impact

Workaround

Fix Status

19.Several data retention information in the Register TRM are incorrect.

Problem Definition

Parameters Affected

Trigger Condition(s)

Scope of Impact

Workaround

Fix Status

22.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete

Problem Definition

≤

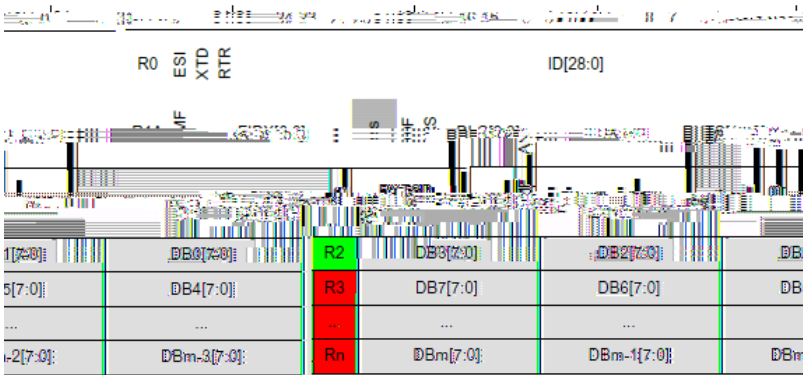


Figure 1 Rx Buffer and FIFO Element

≤ ≤

Figure 2

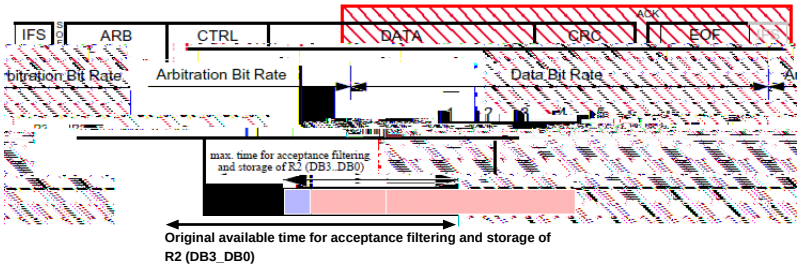


Figure 2 CAN Frame with DLC>4

Parameters Affected

Trigger Condition(s)

≤ ≤

Scope of Impact

Table 1

22.CAN FD sporadic data corruption (payload) in case acceptance filtering does not finish before reception of data R3 (DB7..DB4) is complete	
Workaround	**Table 1** **1)** **Table 1** ≥ **Note:** **2)** **“Trigger Conditions”**
Fix Status	
Impact on Infineon software	*Can_PBcfg.h*

Revision history

Document revision	Date	Description of changes
		Features Features list Blocks and functionality Functional description Electrical specifications Electrical specifications Ordering information Packaging Package Characteristics
		Ordering information Electrical specifications
		Features list Peripheral I/O map Pin assignment Alternate function pin assignments Functional description Trigger multiplexer Interrupts and wake-up assignments HSIOM connections reference Electrical specifications Errata
		Features Features list Functional description Peripheral I/O map Alternate function pin assignments Interrupts and wake-up assignments Core interrupt types Peripheral clocks Peripheral Protection Unit Fixed Structure Pairs Bus masters Miscellaneous configuration Table 26-21 Table 26-24 Ordering information Packaging Appendix

CYT2B7 address map
Functional description t1nt(B
Peripheral I/O map
Package Characteristics U- Tw[u1(a)-18r(Re)-1e5(o
Errata
Ordering information

Block diagram
Functional descrrreon

Updated

Revision History Change Log

Rev. *K Section Updates

Section	Change Description	Current Spec (Rev. *J)	New Spec (Rev. *K)	Reason for change

Rev *K Electrical Specification Updates

Spec ID	Description	Changed Item	Current Spec (Rev. *F)	New Spec (Rev. *G)	Reason for Change
				≤	
				≤ ≤	

Trademarks

IMPORTANT NOTICE

Edition 2023-07-12
Published by
Infineon Technologies AG
81726 Munich, Germany

www.infineon.com

WARNINGS

© 2023 Infineon Technologies AG.
All Rights Reserved.

Do you have a question about this document?
Go to www.infineon.com/support

Document reference
002-18043 Rev. *K