

Copyright

z CAN

z External Interrupts

- Edge or Level sensitive
- Interrupt mask and pending bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

z Non Maskable Interrupt

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

z I/O Ports

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I^2C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GP-IO-pin (either Automotive or CMOS-Schmitt trigger)
- Bit-wise programmable pull-up resistor

z Built-in OCD (On Chip Debugger)

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels
- Execution time measurement function
- Trace function: 42 branches
- Security function

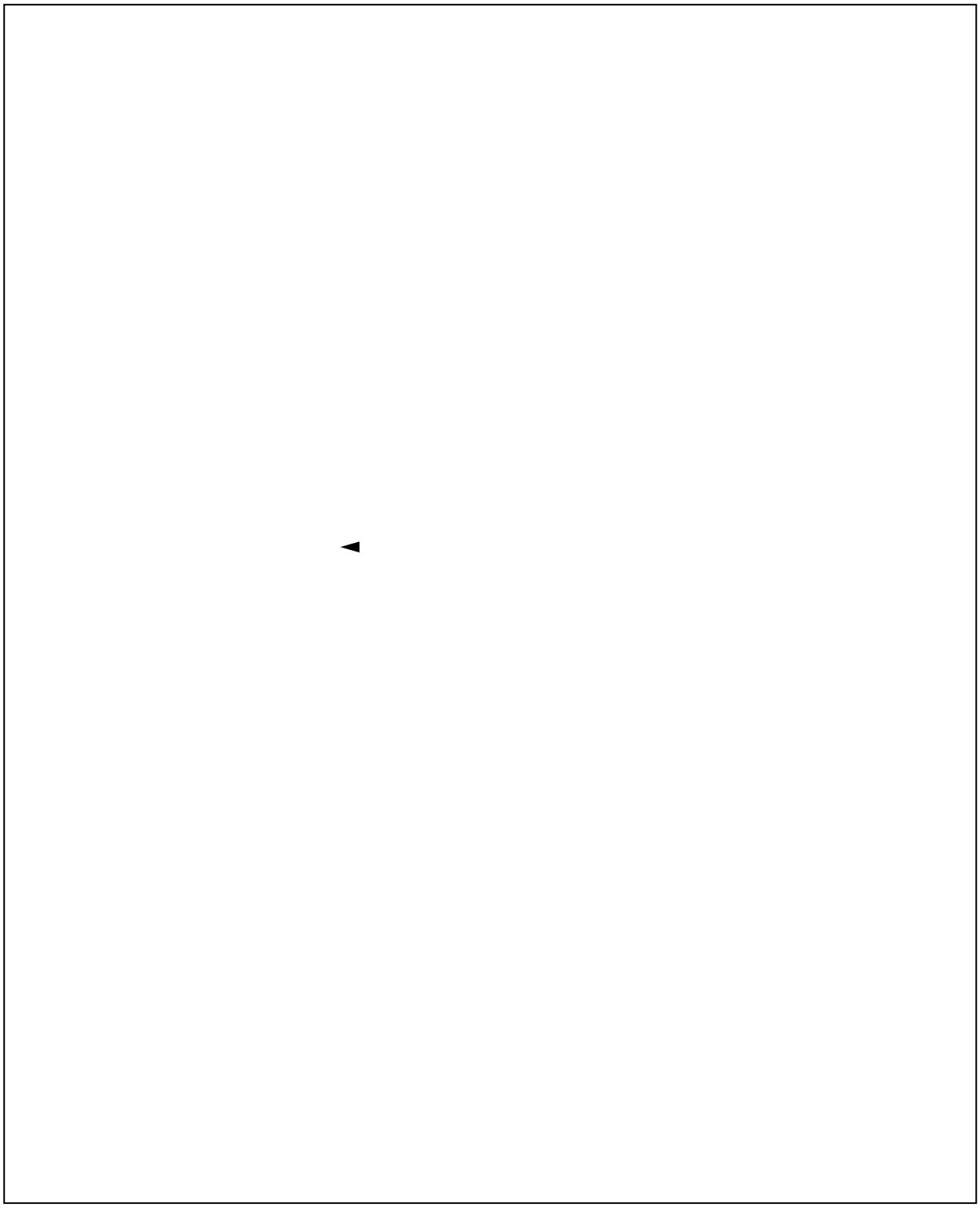
z Flash Memory

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase

PRODUCT LINEUP

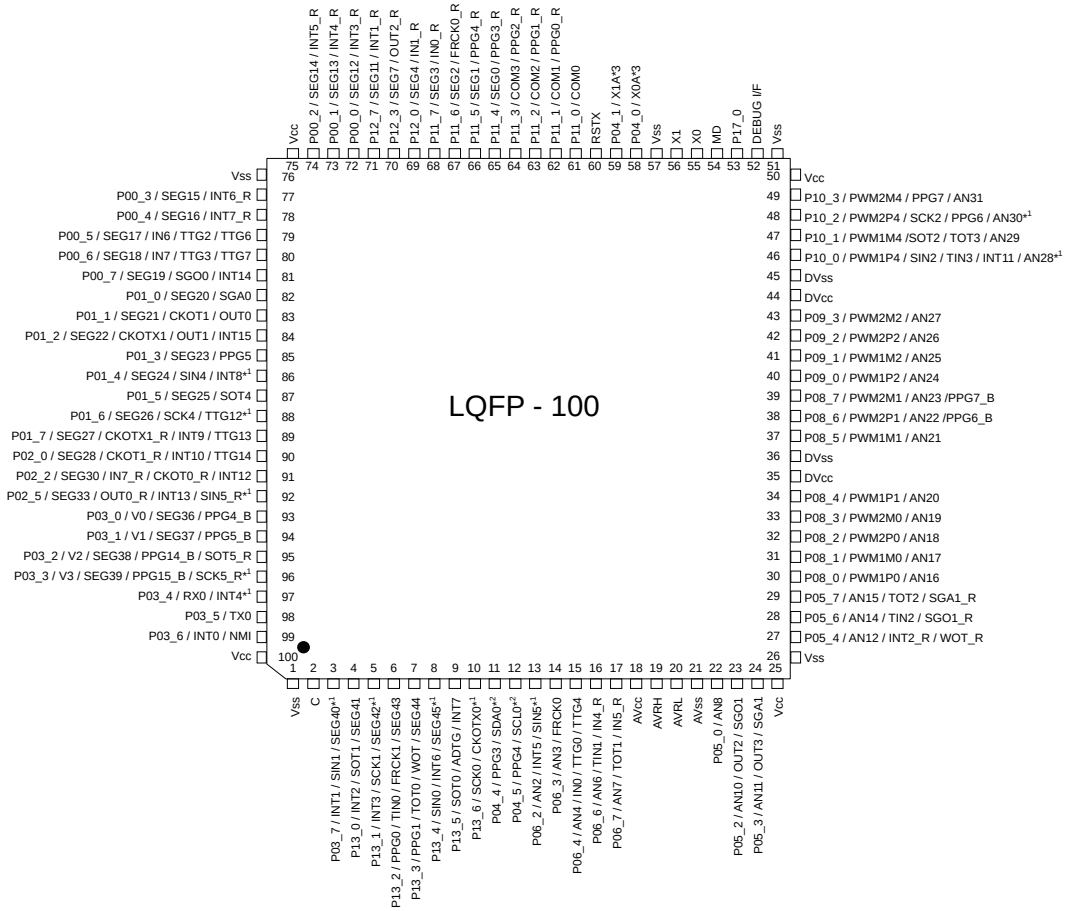
・These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

BLOCK DIAGRAM



PIN ASSIGNMENTS

(TOP VIEW)



(FPT-100P-M20)

*1: CMOS input level only
*2: CMOS input level only for I^2C
*3: Please set Rom Configuration Block (RCB) to use the subclock
All other general-purpose pins have only Automotive input level.

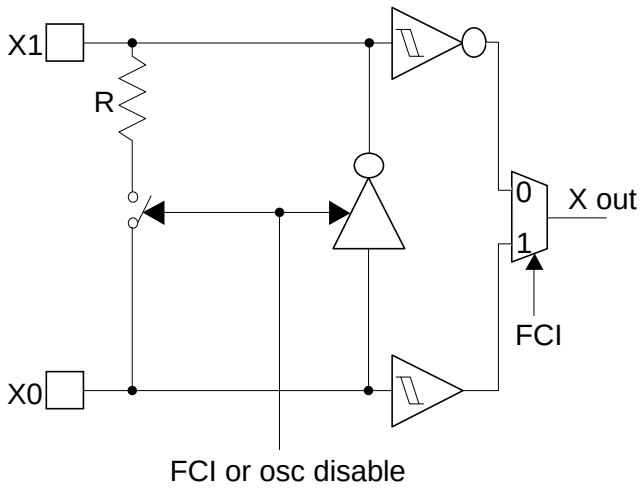
PIN FUNCTION DESCRIPTION

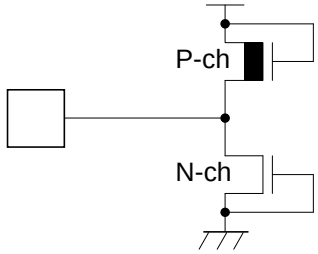
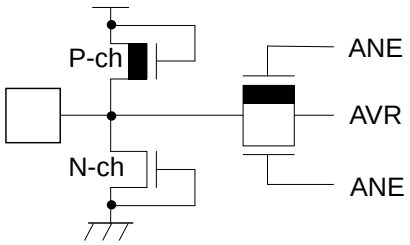
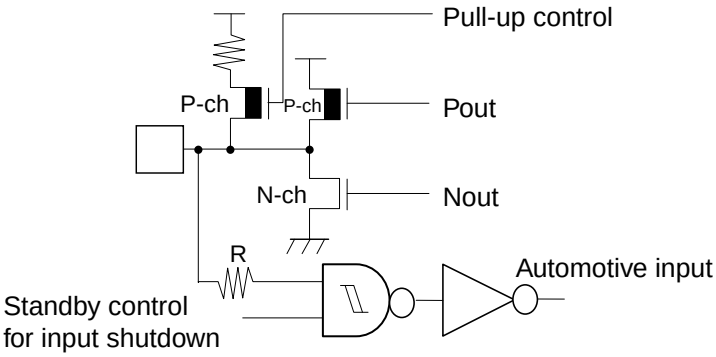
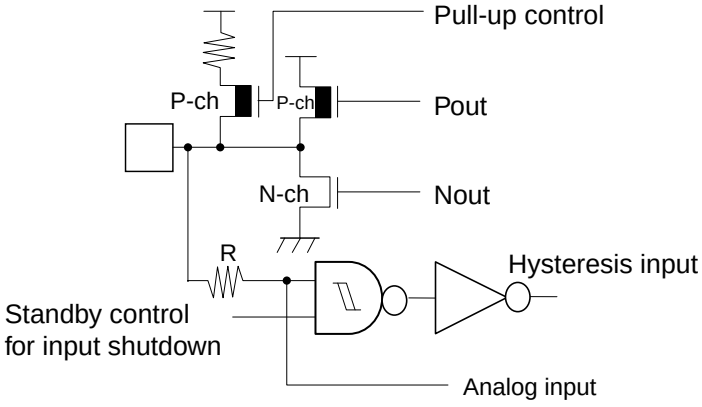
Pin name	Feature	Description
ADTG	ADC	A/D converter trigger input

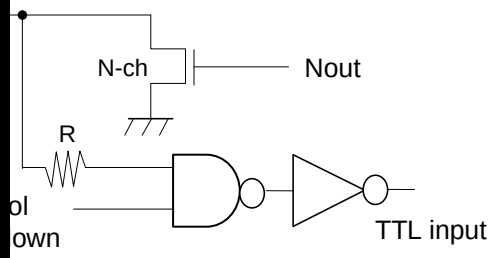
Pin name	Feature	Description
TIN n	Reload Timer	Reload Timer n event input
TOTn	Reload Timer	Reload Timer n output
TTGn	PPG	Programmable Pulse Generator n trigger input
TXn	CAN	CAN interface n TX output
Vn	LCD	LCD voltage reference
Vcc	Supply	Power supply
Vss	Supply	Power supply
WOT	RTC	Real Time clock output
WOT_R	RTC	Relocated Real Time clock output
X0	Clock	Oscillator input
X0A	Clock	Subclock Oscillator input
X1	Clock	Oscillator output
X1A	Clock	Subclock Oscillator output
DEBUG I/F	OCD	On Chip Debugger input/output

Pin no.	I/O circuit type*	Pin name
36	Supply	DVss
37	R	P08_5 / PWM1M1 / AN21
38	R	P08_6 / PWM2P1 / AN22 / PPG6_B
39	R	P08_7 / PWM2M1 / AN23 / PPG7_B
40	R	P09_0 / PWM1P2 / AN24
41	R	P09_1 / PWM1M2 / AN25
42	R	P09_2 / PWM2P2 / AN26
43	R	P09_3 / PWM2M2 / AN27
44	Supply	DVcc
45	Supply	DVss
46	S	P10_0 / PWM1P4 / SIN2 / TIN3 / INT11 / AN28
47	R	P10_1 / PWM1M4 / SOT2 / TOT3 / AN29
48	S	P10_2 / PWM2P4 / SCK2 / PPG6 / AN30
49	R	P10_3 / PWM2M4 / PPG7 / AN31
50	Supply	Vcc
51	Supply	Vss
52	O	DEBUG I/F
53	H	P17_0
54	C	MD
55	A	X0
56	A	X1
	Supply	Vss

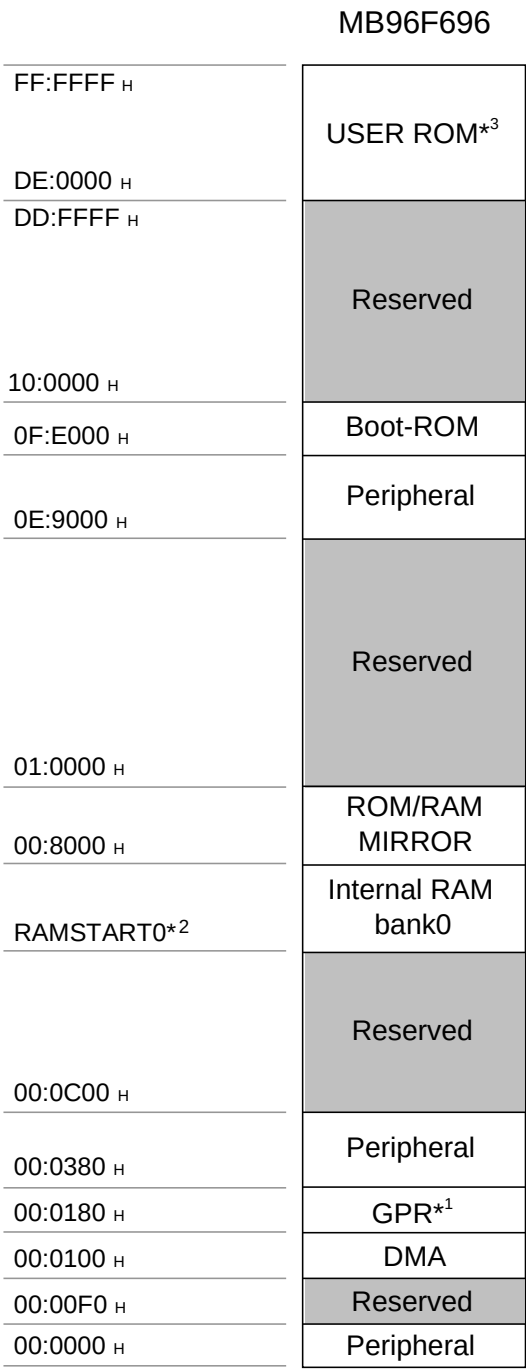
I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		High-speed oscillation circuit: · Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) · Feedback resistor = approx. 1.0 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode · The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
F		• Power supply input protection circuit
G		• A/D converter ref+ (AVRH) power supply input pin with protection circuit • Without protection circuit against V_{CC} for pins AVRH
H		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • Automotive input with input shutdown function • Programmable pull-up resistor
I		· CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) · CMOS hysteresis input with input shutdown function · Programmable pull-up resistor • Analog input

Type	Circuit	Remarks
M		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor
N		• CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor *: N-channel transistor has slew rate control according to I^2C spec, irrespective of usage.
		• I_{OL}: 25mA @ 2.7V • TTL input

MEMORY MAP



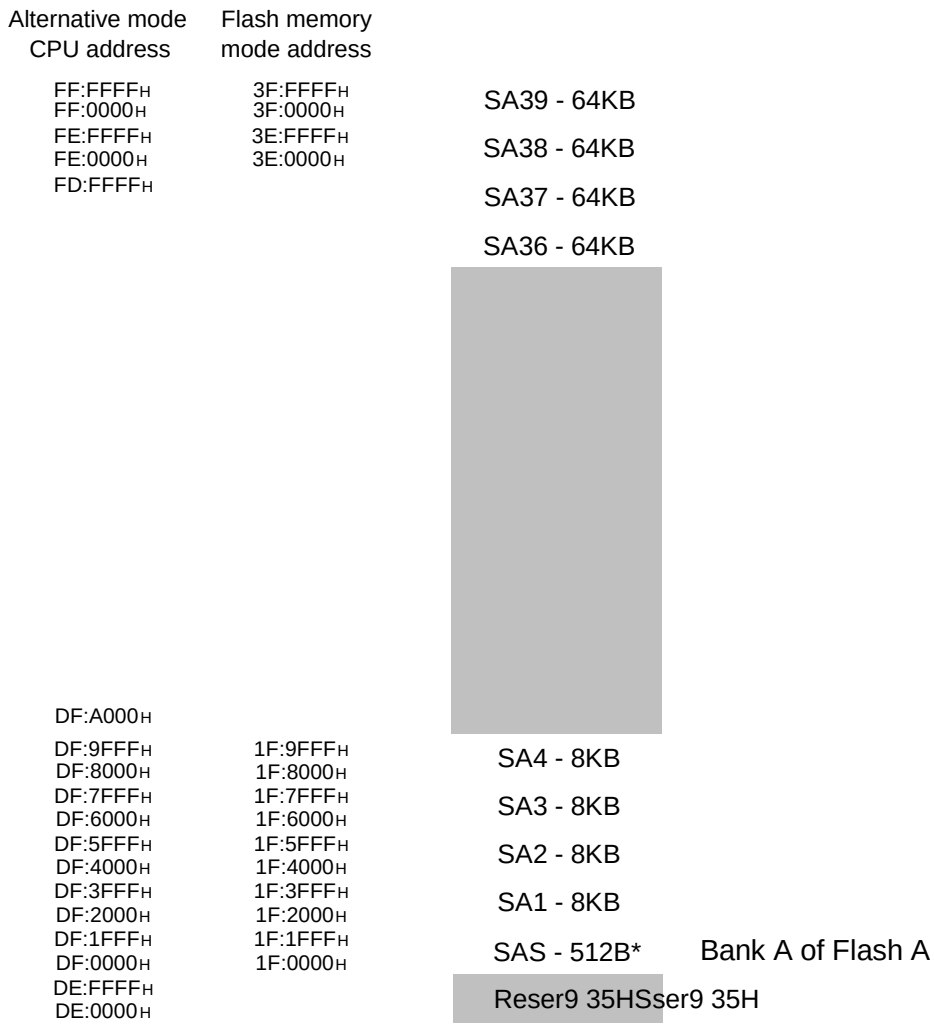
*1: For details about USER ROM area, see the "■USER ROM MEMORY MAP FOR FLASH DEVICES" on the following pages.
*2: For RAMSTART/END addresses, please refer to the table on the next page.
*3: Unused GPR banks can be used as RAM area.

leaourcTc 0.0017 Tw 0 -1.201 MA [area av 0 TcE 0.SM1

RAMSTART ADDRESSES

Devices	Bank 0 RAM size	RAMSTART0
MB96F696	16KByte	00:4200H

USER ROM MEMORY MAP FOR FLASH DEVICES



SERIAL PROGRAMMING COMMUNICATION INTERFACE

		SIN0
9		SOT0

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	2B8	-	-	81	Reserved
82	2B4	-	-	82	Reserved
83	2B0	-	-	83	Reserved
84	2AC	-	-	84	Reserved
85	2A8	-	-	85	Reserved
86	2A4	-	-	86	Reserved
87	2A0	-	-	87	Reserved
88	29C	-	-	88	Reserved
89	298	FRT0	Yes	89	Free Running Timer 0
90	294	FRT1	Yes	90	Free Running Timer 1
91	290	-	-	91	Reserved
92	28C	-	-	92	Reserved
93	288	RTC0	No	93	Real Time Clock
94	284	CAL0	No	94	Clock Calibration Unit
95	280	SG0	No	95	Sound Generator 0
96	27C	IIC0	Yes	96	I^2C interface0
97	278	-	-	97	Reserved
98	274	ADC0	Yes	98	A/D Converter
99	270	-	-	99	Reserved
100	26C	-	-	100	Reserved
101	268	LINR0	Yes	101	LIN USART 0 RX
102	264	LINT0	Yes	102	LIN USART 0 TX
103	260	LINR1	Yes	103	LIN USART 1 RX
104	25C	LINT1	Yes	104	LIN USART 1 TX
105	258	LINR2	Yes	105	LIN USART 2 RX
106	254	LINT2	Yes	106	LIN USART 2 TX
107	250	-	-	107	Reserved
108	24C	-	-	108	Reserved
109	248	LINR4	Yes	109	LIN USART 4 RX
110	244	LINT4	Yes	110	LIN USART 4 TX
111	240	LINR5	Yes	111	LIN USART 5 RX
112	23C	LINT5	Yes	112	LIN USART 5 TX
113	238	-	-	113	Reserved
114	234	-	-	114	Reserved
115	230	-	-	115	Reserved
116	22C	-	-	116	Reserved
117	228	-	-	117	Reserved
118	224	-	-	118	Reserved
119	220	-	-	119	Reserved
120	21C	-	-	120	Reserved

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218	SG1	No	121	Sound Generator 1
122	214	-	-	122	Reserved
123	210	-	-	123	Reserved
124	20C	-	-	124	Reserved
125	208	-	-	125	Reserved
126	204	-	-	126	Reserved
127	200	-	-	127	Reserved
128	1FC	-	-	128	Reserved
129	1F8	-	-	129	Reserved
130	1F4	-	-	130	Reserved
131	1F0	-	-	131	Reserved
132	1EC	-	-	132	Reserved
133	1E8	FLASHA	Yes	133	Flash memory A interrupt
134	1E4	-	-	134	Reserved
135	1E0	-	-	135	Reserved
136	1DC	-	-	136	Reserved
137	1D8	-	-	137	Reserved
138	1D4	-	-	138	Reserved
139	1D0	ADCRC0	No	139	A/D Converter 0 - Range Comparator- 1T /TT0 1

HANDLING DEVICES

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on

2. Single phase external clock for Sub oscillator

- When using a single phase external clock for the Sub oscillator, 'External clock mode' must be selected and X0A/GP04_0 must be driven. X1A/GP04_1 must be configured as GPIO.

4. Notes on PLL clock mode operation

If the PLL clock mode is selected and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

5. Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC}-level as well as all V_{SS}-level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} must be connected to the device from the power supply with lowest possible impedance.

As a measure against power supply noise, it is required to connect a bypass capacitor of about 0.1 µF between Vcc and Vss as close as possible to Vcc and Vss pins.

6. Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board art work surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

7. Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply (AVCC, AVRH, AVRL) and analog inputs (ANn) on after turning the digital power supply (V_{CC}) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case, the voltage must not exceed AVRH or AVCC (turning the analog and digital power supplies simultaneously on or off is acceptable).

8. Pin handling when not using the A/D converter

It is required to connect the unused pins of the A/D converter as AVCC, AVRH = VCC, AVRL = VSS.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	Vcc	-	Vss - 0.3	Vss + 6.0	V	
Analog power supply voltage*1	AVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc*2
Analog reference voltage*1	AVRH, AVRL	-	Vss - 0.3	Vss + 6.0	V	$AV_{CC} \geq AVRH$, $AV_{CC} \geq AVRL$, AVRH > AVRL, $AVRL \geq AV_{SS}$
SMC Power supply*1	DVcc	-	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc= DVcc*2
LCD power supply voltage*1	V0 to V3	-	Vss - 0.3	Vss + 6.0	V	V0 to V3 must not exceed Vcc
Input voltage*1	V_I	-	Vss - 0.3	Vss + 6.0	V	$V_I \leq (D)V_{CC} + 0.3V$*3
Output voltage*1	V_O	-	Vss - 0.3	Vss + 6.0	V	$V_O \leq (D)V_{CC} + 0.3V$*3
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins*4
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	-	25	mA	Applicable to general purpose I/O pins*4
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal outputs
	I_{OLSMC}	T_A=-40°C	-	52	mA	High current outputs
		T_A=+25°C	-	39	mA	
		T_A=+85°C	-	32	mA	
		T_A=+105°C	-	30	mA	
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal outputs
	$I_{OLAVSMC}$	T_A=-40°C	-	40	mA	High current outputs
		T_A=+25°C	-	30	mA	
		T_A=+85°C	-	25	mA	
		T_A=+105°C	-	23	mA	
"L" level maximum overall output current	ΣI_{OL}	-	-	50	mA	Normal outputs
	ΣI_{OLSMC}	-	-	260	mA	High current outputs
"L" level average overall output current	ΣI_{OLAV}	-	-	25	mA	Normal outputs
	$\Sigma I_{OLSMCAV}$	-	-	170	mA	High current outputs
"H" level maximum output current	I_{OH}	-	-	-15	mA	Normal outputs
	I_{OHSMC}	T_A=-40°C	-	-52	mA	High current outputs
		T_A=+25°C	-	-39	mA	
		T_A=+85°C	-	-32	mA	
		T_A=+105°C	-	-30	mA	
"H" level average output current	I_{OHAV}	-	-	-4	mA	Normal outputs
	$I_{OHAVSMC}$	T_A=-40°C	-	-40	mA	High current outputs
		T_A=+25°C	-	-30	mA	
		T_A=+85°C	-	-25	mA	
		T_A=+105°C	-	-23	mA	
"H" level maximum overall output current	ΣI_{OH}	-	-	-50	mA	Normal outputs
	ΣI_{OHSMC}	-	-	-260	mA	High current outputs
"H" level average overall output current	ΣI_{OHAV}	-	-	-25	mA	Normal outputs
	$\Sigma I_{OHSMCAV}$	-	-	-170	mA	High current outputs

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = DV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	Vcc, DVcc	2.7	-	5.5	V	
Smoothing capacitor at C pin	C_S	0.5	1.0	1.5	µF	(Target value) 1.0µF (Allowance within ± 50%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than Cs.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within sponse of o wi743 0.48 9bh75256idx6at is

3. DC Characteristics

1. Current rating of MB96F696 (Target value)

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
	I_{CCPLL}		PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 =32MHz (CLKRC and CLKSC stopped)	-	28.5	-	mA	T_A = +25°C
				-	-	38	mA	T_A = +105°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz (CLKPLL, CLKSC and CLKRC stopped)	-	5	-	mA	T_A = +25°C
				-	-	10	mA	T_A = +105°C

(V_{CC} = AV_{CC}

2. Pin characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "oscillation mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "oscillation mode"	Vcc × 0.8	-	Vcc + 0.3	V	
	V_{IHR}	RSTX	-	Vcc × 0.8	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	Vcc - 0.3	-	Vcc + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	Vcc + 0.3	V	TTL Input
"L" level	V_{IL}	Port inputs Pnn_m	-	Vss - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	Vss - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "oscillation mode"	Vss	-	VD × 0.2	V	VD=1.8V±0.15V

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage*	V_{OL4}	4mA type	$4.5V \le Vcc \le 5.5V$ I_{OL} = +4mA	-	-	0.4	V	
			$2.7V \le Vcc < 4.5V$ I_{OL} = +1.7mA					
	V_{OL30}	High Drive type	$4.5V \le Vcc \le 5.5V$ I_{OL} = +52mA	-	-	0.5	V	T_A = -40°C
			$2.7V \le Vcc < 4.5V$ I_{OL} = +22mA					
			$4.5V \le Vcc \le 5.5V$ I_{OL} = +39mA					T_A = +25°C
			$2.7V \le Vcc < 4.5V$ I_{OL} = +18mA					
			$4.5V \le Vcc \le 5.5V$ I_{OL} = +32mA					T_A = +85°C
			$2.7V \le Vcc < 4.5V$ I_{OL} = +14mA					
			$4.5V \le Vcc \le 5.5V$ I_{OL} = +30mA					T_A = +105°C
			$2.7V \le Vcc < 4.5V$ I_{OL} = +13.5mA					
	V_{OL3}	3mA type	$2.7V \le Vcc < 5.5V$ I_{OL} = +3mA	-	-	0.4	V	
Input leak current	I_{IL}	Pnn_m	$Vss < V_I < Vcc$ AVss, AVRL < V_I < AVcc, AVRH	- 1	-	1	µA	Single port pin except high current output I/O for SMC
		P08_m, P09_m, P10_m	$DV_{SS} < V_I < DV_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 3	-	3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	Vcc = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	Vcc = 5.0V	6.25	12.5	25	Ωk	
Pull-up resistance value	R_{PU}	Pnn_m	Vcc = 5.0V ±10%	25	50	100	Ωk	
Pull-down resistance value	R_{DOWN}	P08_m, P09_m, P10_m	Vcc = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than Vcc, Vss, AVcc, AVss, AVRH, AVRL, P08_m, P09_m, P10_m	-	-	5	15	pF	
		P08_m, P09_m, P10_m	-	-	15	30	pF	

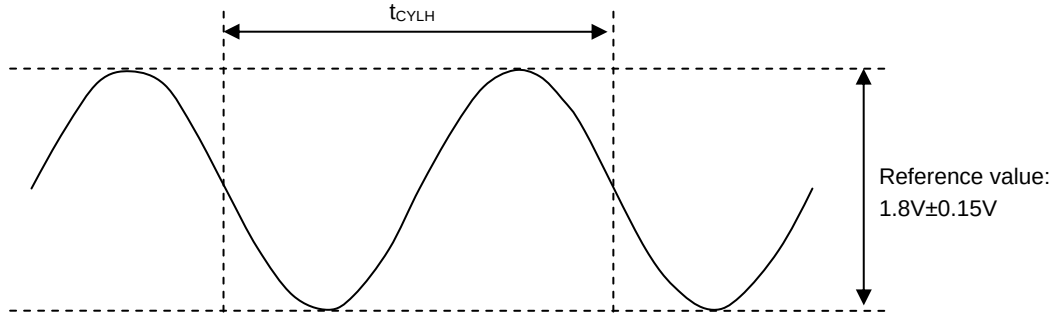
*: I_{OH} and I_{OL} are tarO1c49et value.

4. AC Characteristics

(1) Main Clock Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_{CH}	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	16	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	62.5	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	30	-	70	%	



The amplitude changes by resistance, capacity which added outside or the difference of the device.

(5) Operating Conditions of PLL

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time (LOCK UP time)	t_{LOCK}	1	-	4	ms	Time from when the PLL starts operating until the oscillation stabilizes
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL macro oscillation clock frequency	f_{PLLO}	56	-	108	MHz	

(6) Reset Input Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value	

(8) USART Timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

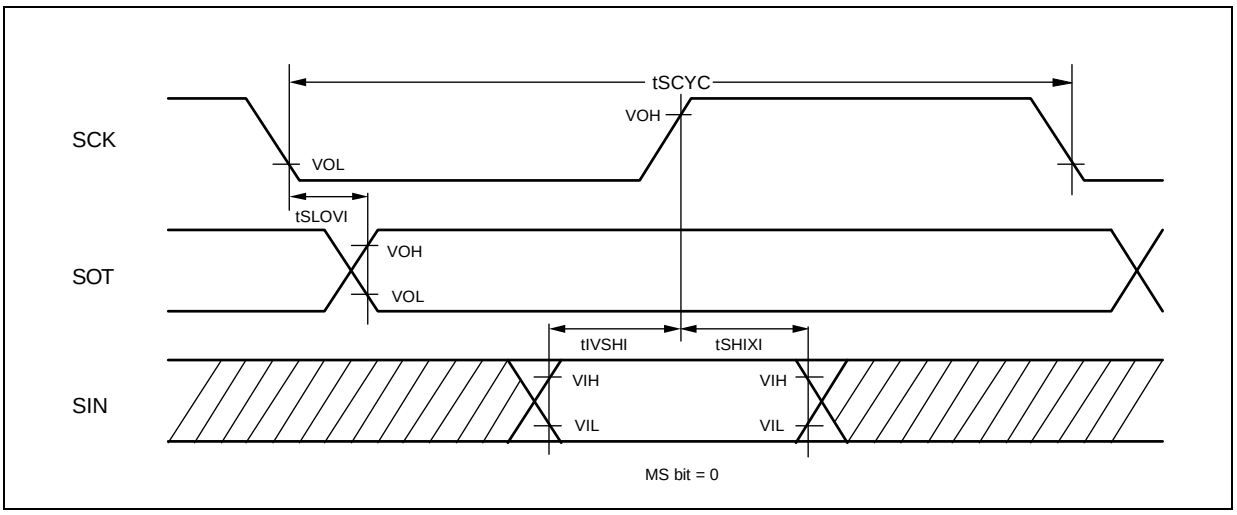
Parameter	Symbol	Pin name	Conditions	4.5V ≤ Vcc < 5.5V		2.7V ≤ Vcc < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	tSCYC	SCKn	Internal shift clock operation	4 t_{CLKP1}	-	4 t_{CLKP1}	-	ns
SCK↓ → SOT delay time	tSLOVI	SCKn SOTn		- 20	+ 20	- 30	+ 30	ns
SOT→ SCK↑ delay time	tOVSHI	SCKn SOTn		N×t_{CLKP1} – 20*	-	N×t_{CLKP1} – 30*	-	ns
SIN → SCK↑ setup time	tIVSHI	SCKn SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK↑ → SIN hold time	tSHIXI	SCKn SINn		0	-	0	-	ns
Serial clock "L" pulse width	tSLSH	SCKn	External shift clock operation	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	tSHSL	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK↓ → SOT delay time	tSLOVE	SCKn SOTn		-	2 t_{CLKP1} + 45	-	2 t_{CLKP1} + 55	ns
SIN → SCK↑ setup time	tIVSHE	SCKn SINn		t_{CLKP1}/2 + 10	-	t_{CLKP1}/2 + 10	-	ns
SCK↑ → SIN hold time	tSHIXE	SCKn SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	tF	SCKn		-	20	-	20	ns
SCK rise time	tR	SCKn		-	20	-	20	ns

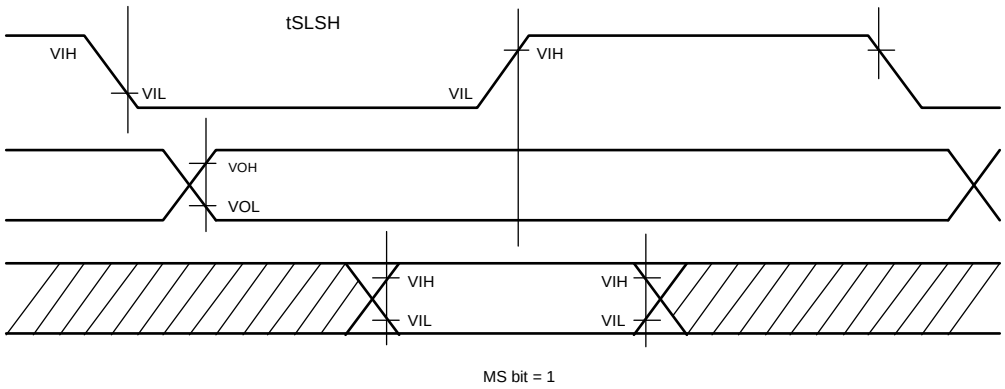
Notes:
- The above characteristics apply to CLK synchronous mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96690 series HARDWARE MANUAL”
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCLKn_0 and SOTn_1 is not guaranteed.

*: Parameter N depends on tSCYC and can be calculated as follows:
• If tSCYC= 2 × k × t_{CLKP1}, then N = k, where k is an integer > 2
• If tSCYC= (2 × k + 1) × t_{CLKP1}, then N = k + 1, where k is an integer > 1
Examples:

tSCYC	N

4 × t_{CLKP1}CLKP1, the5 tCLKP1, the,0.9tCLKP1


tSCYC
SCK
VOH
VOL
tSLOVI
SOT
VOH
VOL
tIVSHI
tSHIXI
SIN
VIH
VIL
VIH
VIL
MS bit = 0

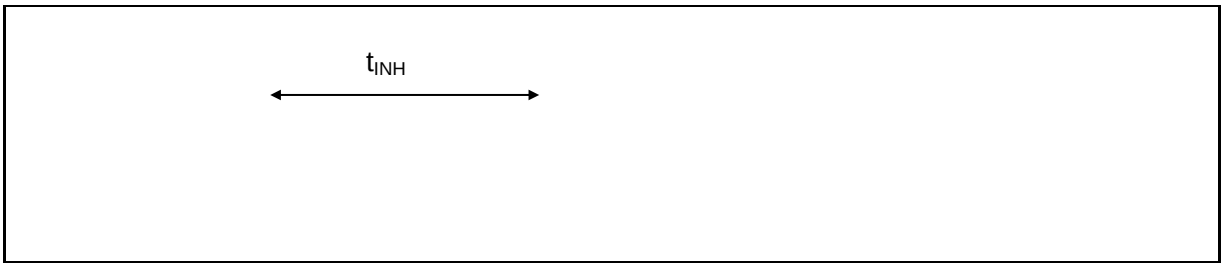

tSLSH
VIH
VIL
VIH
VIL
VOH
VOL
VIH
VIL
VIH
VIL
MS bit = 1

(9) External input timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} t_{INL}	Pnn_m	$2t_{CLKP1}$+200 (t_{CLKP1}= 1/f_{CLKP1})*	-	ns	General Purpose I/O
		ADTG				A/D converter trigger input
		FRCKn, FRCKn_R				Free-Running Timer
		TINn				Reload Timer
		TTGn				PPG Trigger input
		INn, INn_R				Input capture
		INTn, INTn_R, NMI	200	-	ns	External interrupt NMI

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



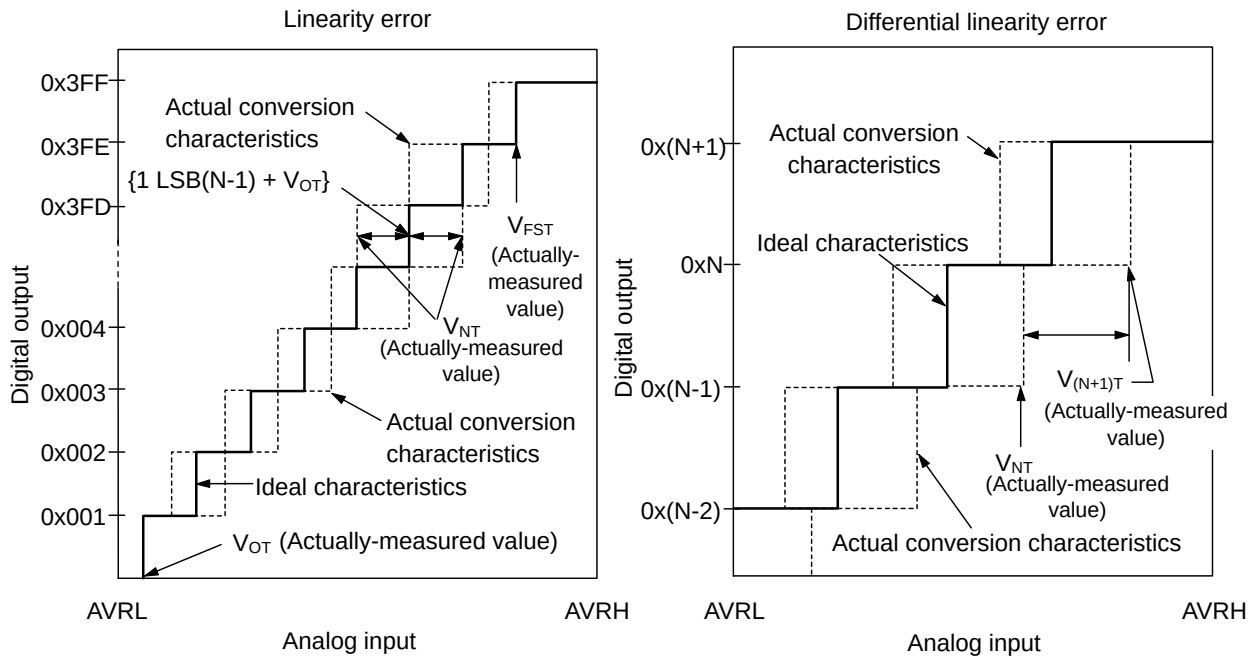
(10) I^2C timing

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	fSCL		0	100	0	400	kHz
(Repeated) START condition hold time SDA↓ → SCL ↓	tHDSTA		4.0	-	0.6	-	µs
SCLclock "L" width	tLOW		4.7	-	1.3	-	µs
SCLclock "H" width	tHIGH		4.0	-	0.6	-	µs
(Repeated) START setup time SCL ↑ → SDA↓	tSUSTA		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA↓ ↑	tHDDAT		0	3.45*2	0	0.9*3	µs
Data setup time SDA↓ ↑ → SCL↑	tSUDAT	o tSUDAT	906006d [2Tc		029.10029.ns297		0

• Definition of 10-bit A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Linearity error : Deviation of the line between the zero-transition point (0b0000000000 0b0000000001) and the full-scale transition point (0b1111111110 0b1111111111) from the actual conversion characteristics.
- Differential linearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and linearity error.

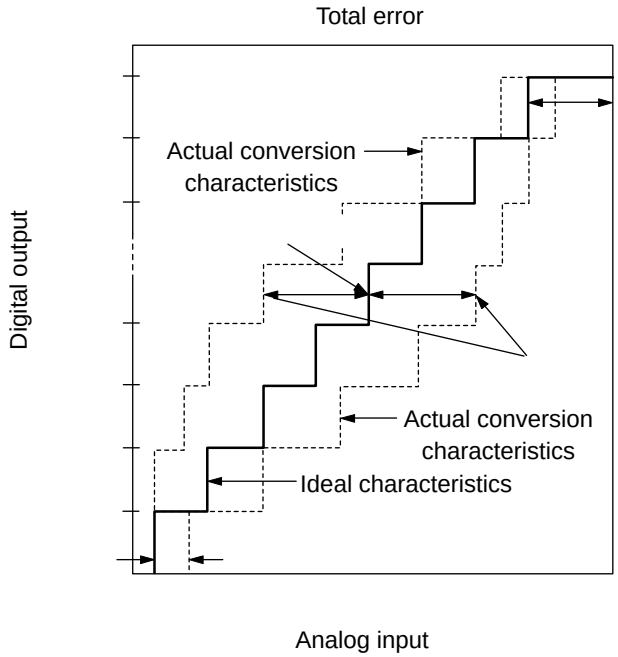


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB'} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N 1) to 0xN.



$$1LSB' \text{ (Ideal value)} = \frac{AVRH - AVRL}{1024} \text{ [V]}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB' \times (N - 1) + 0.5LSB'\}}{1LSB'}$$

N : A/D converter digital output value.
V_{NT} : Voltage at which the digital output changes from 0x(N + 1) to 0xN.
V_{OT}' (Ideal value) = AVRL + 0.5LSB[V]
V_{FST}' (Ideal value) = AVRH - 1.5LSB[V]

z High current output slew rate

(V_{CC} = AV_{CC} = 2.7V to 5.5V, DV_{CC} = 4.5V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Rise time / Fall time	t_{R2}, t_{F2}	P08_m, P09_m, P10_m	15	-	75	ns	C_L=85pF

z 83 15(V899 0 Tj 050 Tc99 444.48 694.3625 366 184340.4_m,)TjSS862(C)]T61 ime V899 0 Tj

z Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = DV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = DV_{SS} = 0V, T_A = - 40°C to + 105°C)

	Value		

ORDERING INFORMATION

Part number	Flash memory	Package
MB96F696RAPMC-GSE1*	Flash A (288.5KB)	100-pin plastic LQFP (FPT-100P-M20)
MB96F696RAPMC-GSE2*		

*: These devices are under development and specification is preliminary.
These products under development may change its specification without notice.

REVISION HISTORY

Revision	Date	Modification
Prelim 1	6-Ju1-2011	Creation

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